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L-Band Solid-State Transmit/Receive Module

Phase-II Final Report
[Unclassified Title]

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Aerospace Systems Branch
Space Systems Division

December 17, 1975

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20. ABSTRACT *(Continue on reverse side if necessary and identify by block number)*

Phase II of a two-phase program to develop solid-state microwave transmit/receive modules has been partially completed. Modules fabricated to exacting mechanical and electrical specification have been received from two of three manufacturers and have been extensively evaluated using a highly sophisticated, computerized test facility at the Naval Research Laboratory. The modules could be interpreted as second-generation engineering models but with many design features of preproduction units. In most cases stringent specifications were achieved.

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CONTENTS

EXECUTIVE SUMMARY

(U) This section summarizes results of tests conducted by the Naval Research Laboratory (NRL) personnel.

(U) The objective of the two phase program was to develop a completely solid state L-band transmitter/receiver module for use as active elements in a phased array.

(U) A module consists of a transmitter, a low-noise RF receiver, a digitally controlled RF phase shifter, an isolator and required T/R switching circuitry, housed in a single container with suitable logic circuitry included such that RF, DC, and logic-control commands only must be applied to the device.

(U) Development was contracted by NRL to three manufacturers:

To complete Phase II each contractor was required to deliver a quantity of working models (5 or 6, dependent on contractor) and a report containing supportive evidence of the modules' capabilities.

(U) Delivery of the devices and completion of the terms of the contract has been completed by RCA and Microwave Associates. Westinghouse has not delivered the required devices as of this report, and data and evaluation of Westinghouse modules is not included. Upon delivery and completion of evaluation, an addendum will be attached to this report.

(U) Tests to verify contractor's results were performed at NRL in an extensive test facility configured for this type of task. The evaluation of the receiver channels was accomplished in a CW mode using a Hewlett-Packard (HP) Automatic Network Analyzer, under computer control. The transmitter channels were evaluated in a pulse mode using an extensively modified Scientific-Atlanta Pulsed Measurement System.

EVALUATION AND ANALYSIS

(U) The module parameters of gain (power output), insertion phase, noise figure, stability, and pulse shape were evaluated over many combinations the variables of commanded phase state (16 discrete conditions), input drive power (transmitter only), frequency, DC supply voltages, and temperature. This data was stored on magnetic tape for future retrieval and processing.

(U) The data was processed to obtain peak, average, and RMS variations with frequency, temperature, and voltage in combinations suitable for further interpretation.

(U) This data was further reduced in reference tables for quick access.

(U) All receivers exhibited gains in excess of the 25 dB minimum for most test conditions. Deviations did occur in linearity of gain (dB bandwidth), especially for the various phase states.

(U) Noise figure of the receivers was exceptionally good and indicated progress in the state of the art.

(U) Receiver phase parameters were typically within specification limits.

(U) Transmit power was quite insensitive to input power (due to class-C operation) and supply voltage. All modules however exhibited maximum power output for maximum voltage and drive, minimum temperature, and at maximum temperature, power output was on occasion marginal.

(U) Some small amount of pulse droop was noted and of such a nature that further stabilization of the input DC voltage was ineffective.

(U) Of the two contractors reported, each designed their own RF circuitry, tuning structures, enclosures, etc. In addition each independently designed any temperature and/or voltage compensation circuitry. Each contractor selected a different source of output transmitter transistors, which were also designed independently.

(U) It is of interest to note that, while specific variations did occur, for all test conditions and modules the average value of the peak power delivered by each contractor was essentially the same (124 watts peak).

CONCLUSIONS:

(U) The program could be considered successful in that a capability

has been demonstrated in the manufacture of all-solid-state modules at L-band.

(U) These devices, however, while constructed to many manufacturing techniques were not production items and did exhibit certain characteristics that must be modified prior to production. Improvement in performance and stability at temperature extremes, capability for storage below -30°C, improvement in logic repeatability below 0°C, immunity to out-of-band RF signals, and fail-safe operation with DC voltages are some areas that merit further investigation.

L-Band Solid-State Transmit/Receive Module
Phase - II Final Report
(Unclassified Title)

1.0 INTRODUCTION

(U) This report encompasses those efforts performed during the period April 15, 1974, to September 15, 1974, to extensively evaluate and categorize the performance parameters of fully hermetic solid-state, transceiver modules designed and produced under Phase II of a program supported by the Space System Division of the Naval Research Laboratory, Code 7947. This phase is an extension of earlier Phase I Module design efforts which resulted in the delivery of two engineering models from the same three contractors noted herein. Phase I efforts were reported earlier in NRL Report 7873.

(U) The measured data provided herein was obtained by the Naval Research Laboratory and although similar to that measured and reported by the module contractors it is intended to provide additional detailed comparison analysis (not heretofore available) among the various developers and to yield information on the present state of the art. In this way, the system designer will have available subsystem information which will result in a more optimum and timely design.

(U) The module specifications were originally prepared for a radar system in an ocean surveillance application. During the course of the module development the radar system design changed significantly. The development was however finished using the original specification (see Appendix I) as a base line with the development goals being to achieve the most the present state of the art would allow.

Manuscript submitted October 30, 1975.

(U) The measured module data thus obtained has been retained in a form compatible with computer processing. In this unprocessed form, this data contains all information supplied in this report, in addition to having the potential for further evaluation and comparison depending upon future systems needs.

(U) With the exception of special receiver parameter tests, such as noise figure and gain compression, all data noted herein was obtained using a computerized control and storage system. Parts of this NRL module test facility are made up of standard laboratory test equipment; however, the complete facility includes a sizeable amount of special equipment designed at NRL for the specific purpose of obtaining and processing large quantities of microwave data rapidly. Extensive computer programming has been accomplished to yield specialized but varied testing. Included as part of this report is a description of the test facility with descriptions of the novel techniques employed to process data for clear and concise evaluation.

1.1 PROGRAM SCOPE AND OBJECTIVES

(U) The program effort described in this report includes the technical support of Naval Research Laboratory personnel. However, the transceiver modules evaluated were produced by outside contracts as follows:

RCA Corp.
Moorestown, N. J. Contract No. N00014-72-C-0212

Microwave Associates, Inc. (MA)
Burlington, Mass. Contract No. N00014-72-C-0213

Westinghouse
Baltimore, Md. Contract No. N00014-72-C-0214

At the time of this report, two contractors, RCA and MA have each delivered transceiver modules, allowing sufficient time for thorough NRL evaluation. Westinghouse has encountered technical difficulties relating to transistors and has not delivered modules although some intermediate sampling has been performed at NRL.

(U) Therefore, this report includes data and an evaluation of RCA and MA modules and will be updated by means of an addendum when Westinghouse module data is available.

(U) Prime program objectives are:

A. To design and thoroughly test L band, RF solid state, transceiver modules containing:

a. microwave receiver

b. microwave transmitter

c. necessary transmit-receive switching functions to obtain controlled operation.

d. diode switched reciprocal line length phase shifter located such that it is part of either the transmitter or receiver channel

e. some specialized electronic control circuitry necessary to the specific operation of each transceiver independent of all others of the same class.

B. To evaluate initial transceivers and from the data obtained, subsequently engage in a design improvement and productization program to minimize defects in second generation units. (Phase II of this program).

C. To extensively evaluate and process the measured module data in an optimum manner such that performance trends and statistics can be obtained and to retain this data in a form suitable for other specialized evaluation as required.

2.0 THE SOLID STATE TRANSCEIVER

(U) The concept of a single microwave transceiver plug-in package is not new. It has in the past been restricted to low power or to applications where size of a single package was practical. Therefore the transceiver concept was not typically applied to radar applications until the practical development of active element phased array systems. But even with the advent of phased arrays, the transceiver concept required the development of all-solid-state microwave integrated circuit components to minimize size with additional goals of cost reduction, improved efficiency, and reliability. In addition the elemental module concept was slightly modified from many former non-radar applications in that the transceiver transmitter now became an amplifier with precise phase and amplitude characteristics rather than just a simple source of RF energy.

2.1 MODULE EVOLUTION

(U) The units produced and described in this report are the result of a long and sometimes arduous process of engineering design and development that is dependent not only on advances in microwave integrated circuitry, but also on the availability of specialized microwave transistors capable of delivering sizeable peak powers (for transmit operation), or low noise figure (for receive operation).

(U) The day of the high power (for this application approximately 30-40 watts peak) transistor was ushered in by the use of chip cell design wherein each semiconductor device included multiple quasi-

independent cells operating in parallel. This permitted improved thermal dissipation properties and when combined with techniques of input and output circuit matching as part of the transistor package (chip carrier concept) yielded a useful and "reasonably" reproducible device.

(U) The resultant microwave subassemblies including receiver and 100 watt (minimum) peak power transmitter are shown in Figures 1 and 2. The devices pictured are those units delivered as part of the Phase-II endeavor. Modules were competitively procured from multiple sources based upon the assumption that no single module contractor nor any one transistor manufacturer was exclusively endowed with expertise and module "know-how" in a field of endeavor which is currently undergoing extremely rapid advances in technology.

(U) High-power transistors employed in these modules are similar to those seen in Figures 3a, 3b, and 3c. Protective covers have been removed to show the multi-cell and chip carrier design concept, thus providing a better understanding of the technology involved.

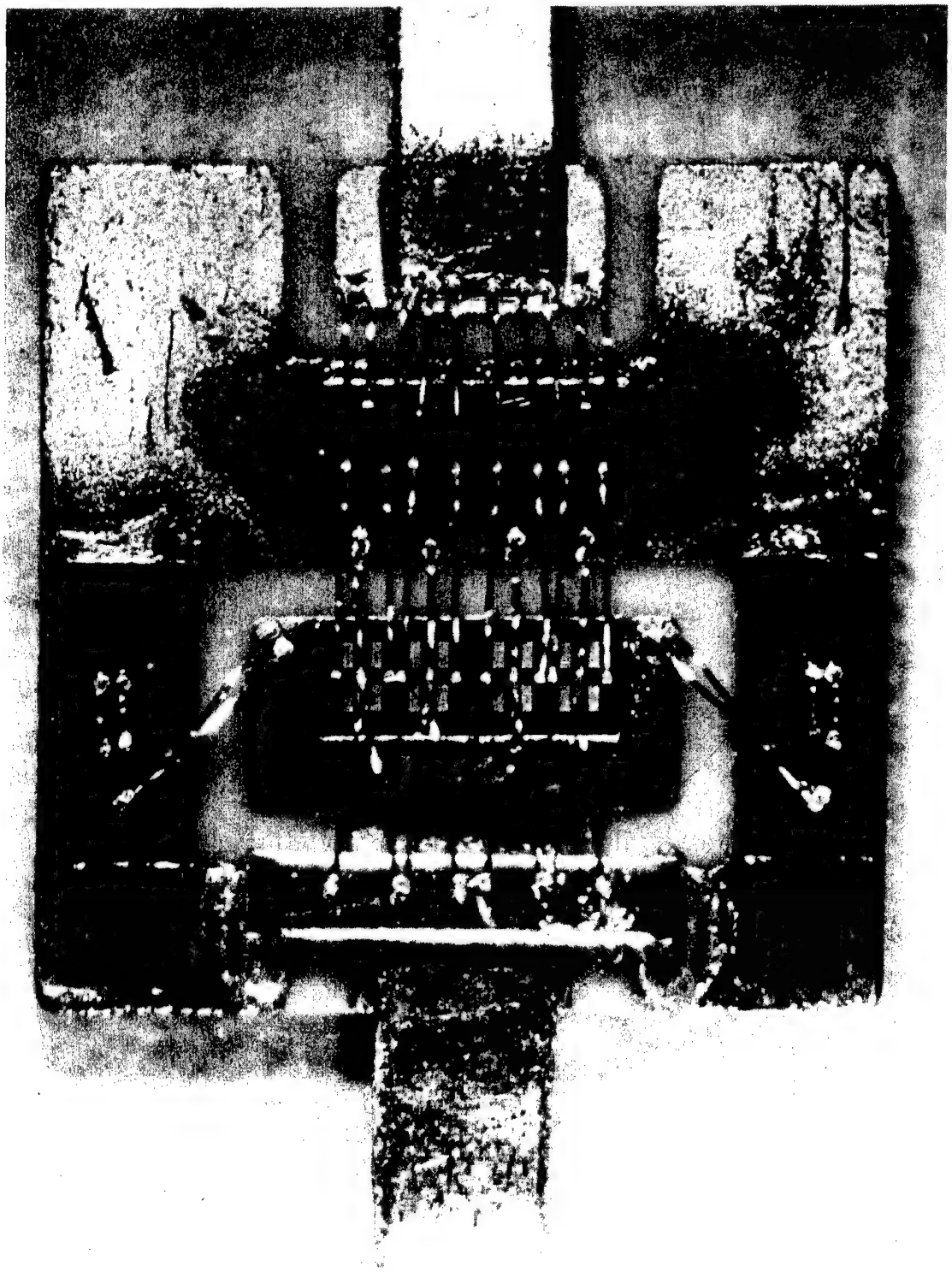
2.2 DETAIL CIRCUITRY

(U) Figure 4 is a typical block diagram of the transceiver showing the major building blocks. This diagram is for illustrative purposes only and is not intended to depict precisely the number of stages in any given module design. In the receive mode, signals received into the antenna port pass through the circulator to the low noise receiver. This receiver consists of multiple stages of amplification such that overall module gain in the receive mode is 25 dB minimum. After RF

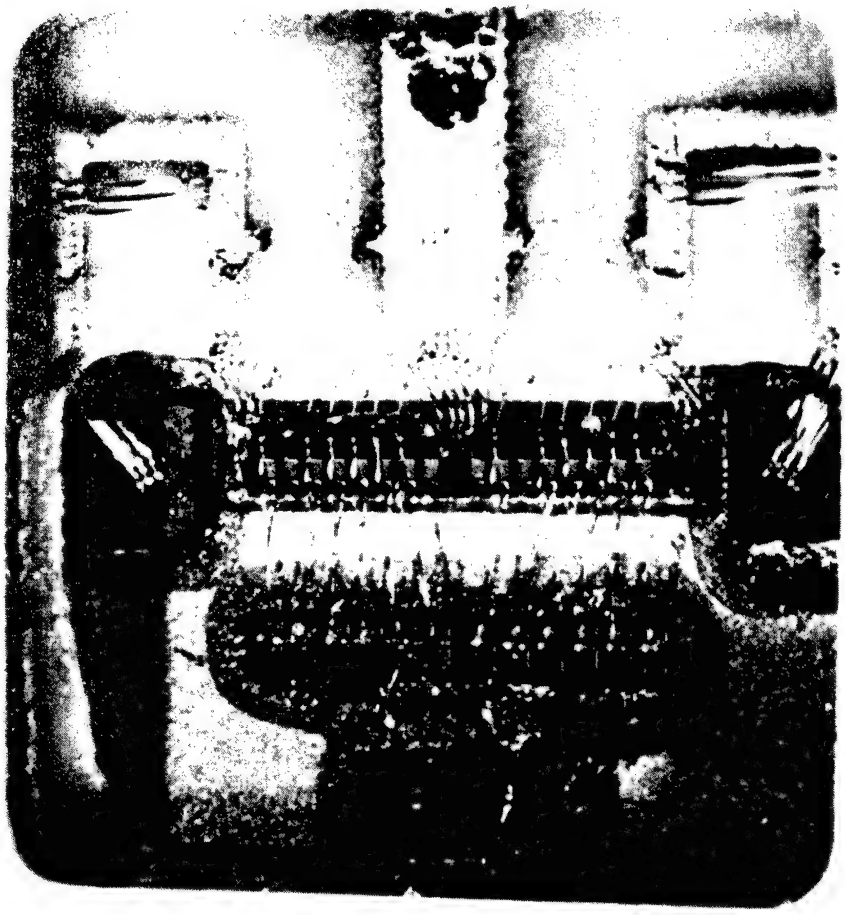
(U) Fig. 1 - Internal and external views of RCA Phase-II microwave transceiver module (internal view includes high-power and driver transistors)

(U) Fig. 2 - Internal and external views of Microwave Associates transceiver module (internal view includes receiver, phase shifter, and logic)

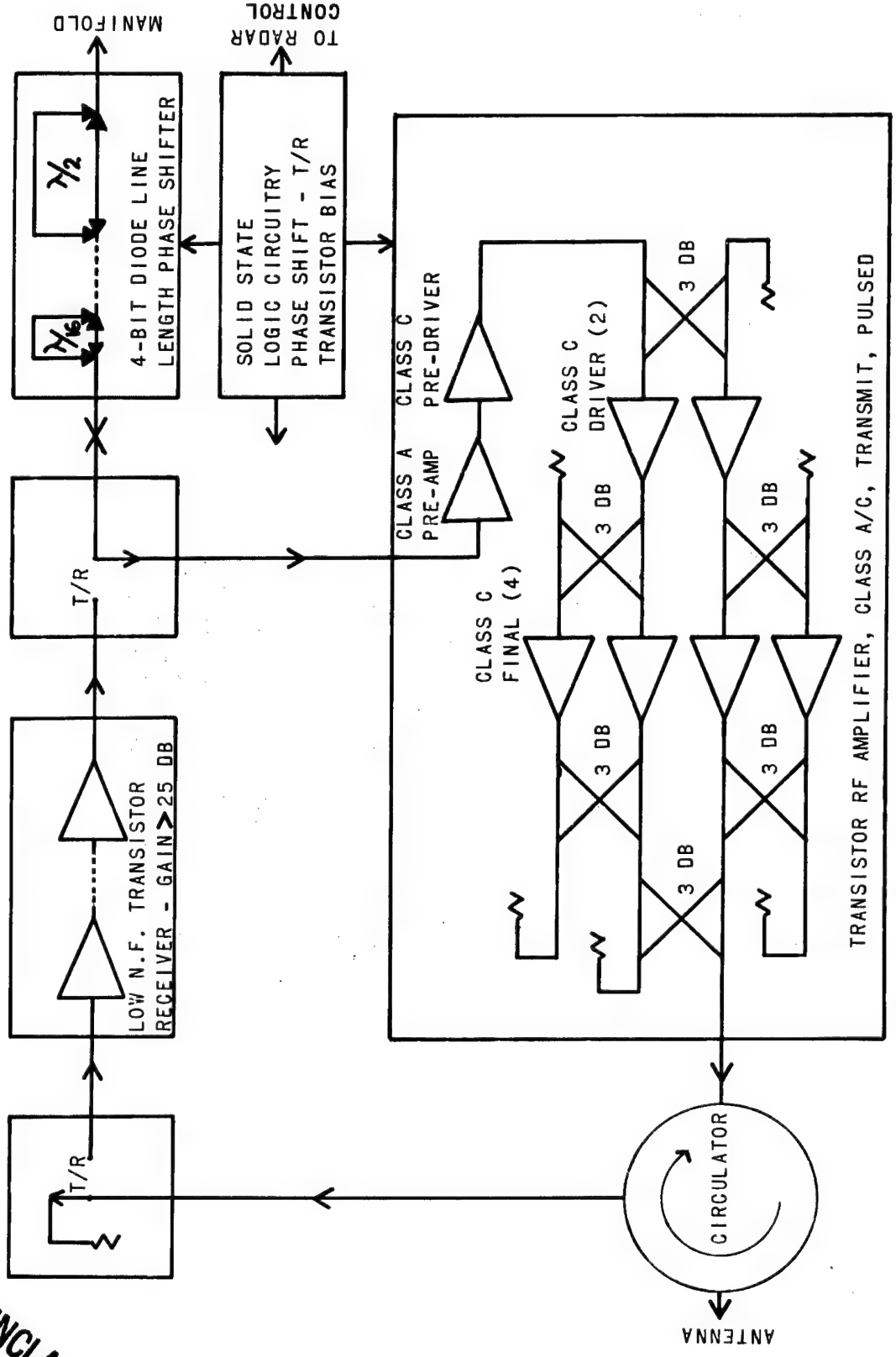
(U) Fig. 3a - Power transistor, MSC 1330B, showing cell construction



(U) Fig. 3b - Power transistor, PHI 1520, showing chip carrier design



(U) Fig. 3c - Power transistor, MSC "AMPAC", showing chip carrier design



(U) Fig. 4 - L-band solid-state transceiver module

amplification, the signal is fed through a 4-bit-diode-line-length phase shifter and out of the module via the "manifold port". This connection is referred to as the "manifold port" because it is the interface between the module and the RF manifold or feed network in a phased array application. Phase-shifter bits (line lengths) are selected by video logic commands. Decoding logic networks are included to convert serial input data into 4-bit binary logic necessary to drive the sixteen phase-shifter diodes and T/R switches.

(U) For transmit operation, RF drive signals from the system manifold first pass through the reciprocal-line-length phase shifter in the opposite direction from the receive-mode path previously described. Signals are then amplified through several cascaded transistor amplifier stages. The first stage is usually operated class A and application of the collector voltage is also sometimes controlled by the T-R (transmit-receive) switch logic to conserve dc power and thereby improve overall module efficiency.

(U) Due to magnitude of the required output power level, four parallel power transistors are employed in the final output stage. These transistors are operated class C with essentially zero standby current to maximize efficiency without the requirement of additional dc switching circuitry. Because of matching requirements and gain limitations, two additional transistors are incorporated as drivers for the final stage with one transistor included as class C predriver.

(U) To provide maximum isolation at both the input and output of each of the parallel final transistors, matched 3-dB couplers are employed which typically exhibit in excess of 20 dB isolation over the desired

band of interest. Any amplitude or phase differences (errors) generated among the various transistors is absorbed in the load balancing RF terminations and thus not reflected back to the individual output transistors.

(U) After amplification, the rf signal is directed through a T-R switch and a circulator to the output (antenna) port; depending on module thermal design and external heat sink capacity, four output power transistors operating in parallel, can practically deliver a minimum of 100 watts peak for pulse widths up to several milliseconds at a typical duty factor of 12%. Because of thermal design limitations, the modules produced and evaluated during this program operated under somewhat less stringent pulse width conditions (several hundred micro-seconds).

3.0 TEST AND EVALUATION CRITERIA

(U) Because of the number of parameters of importance and the varied test conditions to be investigated, it is customary to only spot check a module under investigation. While this method is often acceptable to attain a reasonable assurance of quality and conformance it is nevertheless insufficient when the purpose of evaluation includes the derivation of sufficient statistical data to determine trends and working knowledge of the limitations of the modules, independent of certain specification requirements.

(U) The specification governing the basic design of the transceiver module is included for reference in Appendix I of this report. This document was intended primarily as a module design guideline. In testing of the resultant units, this specification was used only as a base line for evaluation.

(U) As definitions and interpretations were modified to include the latest inputs from the various disciplines involved, the evaluation procedures were also allowed to change to optimum advantage. These changes in emphasis resulted in corresponding changes in software and hardware throughout the program which is evidenced in the number of iterations in software necessary to obtain maximum benefit from the collected data and the number of modifications and additions to hardware incorporated into the test system for test parameter control.

(U) NRL test facility included a Hewlett-Packard Automatic Network Analyzer and a Scientific Atlanta Pulsed Measurement Receiver with special support equipment for complete computer control. This equipment is shown in Figure 5.

(U) Fig. 5 - NRL module test facility

3.1 RECEIVER MEASUREMENT AND DATA PROCESSING

(U) With the exception of noise figure and gain compression, all module measurements in the receive mode were made under small-signal, CW, RF test conditions using a Hewlett-Packard 8542 Automatic Network Analyzer. A HP 2100 computer was employed for digital control, and likewise used with the Scientific-Atlanta pulse measuring equipment when evaluating modules in the transmit mode. This same computer facility was also used throughout the program for processing module data.

(U) Each transceiver was evaluated under the following test conditions, the results of which are reported in Section 4:

a. 3 temperatures ($-30^{o}C$, $+20^{o}C$, $+70^{o}C$)

b. 3 voltages (-2%, nominal, +2%)

c. 41 frequencies in 5-MHz steps

d. 16 phase states (4-bit phase shifter)

e. Measure S parameters S_{11} and S_{21} and store on tape.

The raw data thus obtained can be processed, as required, to obtain the desired specific performance properties.

(U) The data has presently been processed to yield:

a. VSWR and gain vs frequency, for each temperature, voltage, phase state.

b. Insertion phase deviation from linear and quadratic, RMS error of insertion phase from linear, maximum peak error, and equivalent length of air line and phase offset that this insertion phase represents; for each temperature, and voltage with bit 0 defined as the insertion phase state.

c. Differential phase error vs frequency as compared to the desired value with bit 0 defined as the reference state; for each temperature, voltage, and phase state.

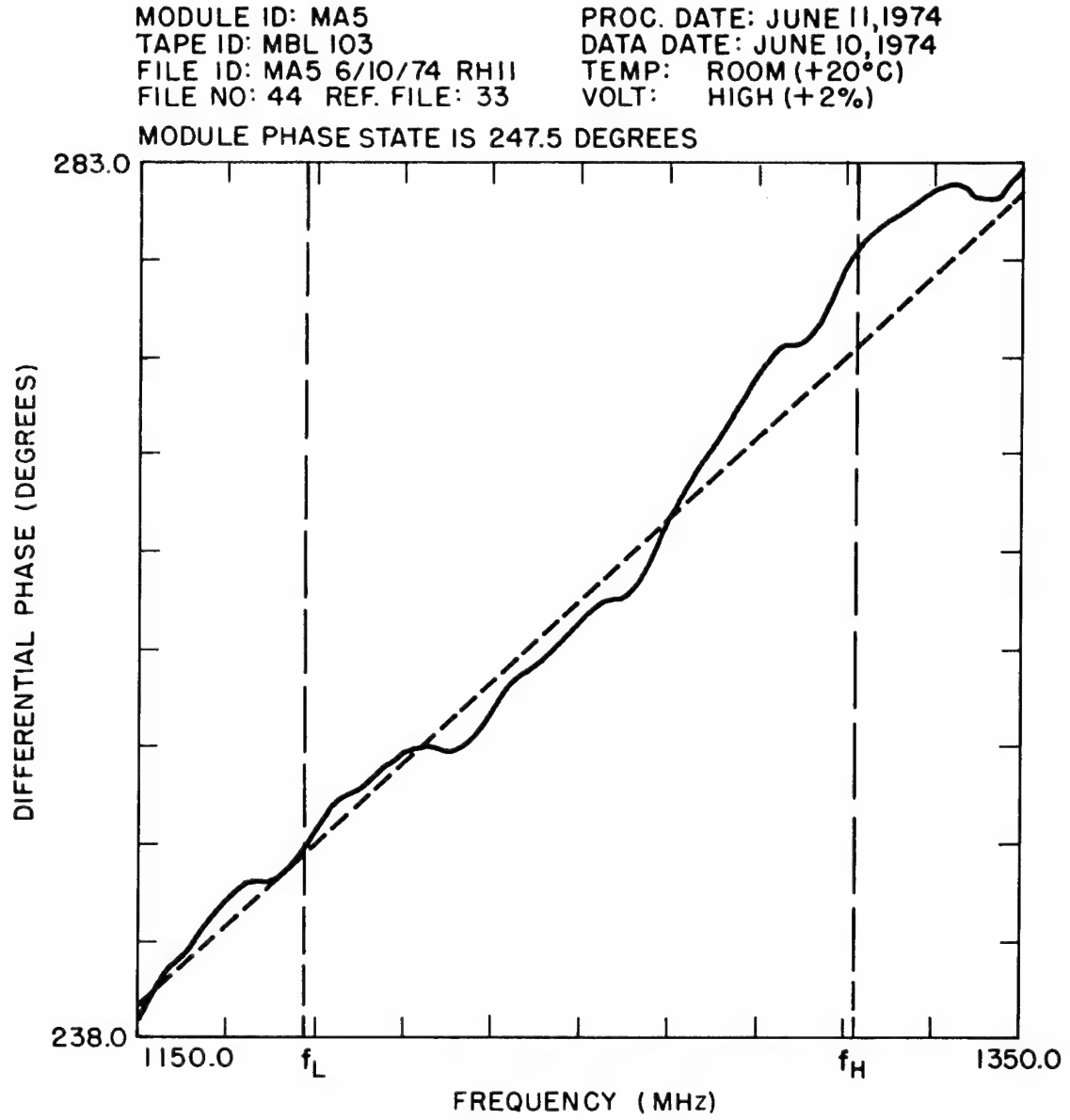
d. Maximum/minimum gain, VSWR, and differential phase error, for each temperature and voltage over all phase states.

e. RMS differential phase error; for each temperature and voltage over all phase states and frequencies.

f. Histograms of numbers of samples vs magnitude of differential phase error and variation in gain from average; for each temperature and voltage over all phase states and frequencies.

(U) For each transceiver there is therefore not only a large mass of data representing individual test conditions but also for each general category of temperature and voltage there is an additional set of summary data (9 such sets of summary data exists for each transceiver). To illustrate, Figure 6 is a typical page of data resulting from the evaluation of the receiver channel of a particular Microwave Associates module. Due to this large quantity of data it is not practical to even include the summary sheets which would be in excess of 90 pages for each module tested. Data will therefore be reduced into a concluding table so as to permit a subsequent discussion of the various parameters investigated. In this way, general trends, including those unit to unit parameters of interest can be highlighted.

(U) Noise figure and gain compression were evaluated using manual laboratory equipment; there was no attempt to automate these particular tests for the limited scope of this particular program.



(S) Fig. 6 - Typical receiver channel data - (Mircowave Associates #5)

3.2 TRANSMIT MEASUREMENT AND DATA PROCESSING

(U) As was the case with receive measurements, the quantity of data necessary to perform meaningful statistical analyses and trend evaluations is enormous. To undertake such a test program using manual equipment is quite impractical.

(U) The pulse measurement system employed was originally developed at Scientific Atlanta and subsequently modified at NRL to include: synchronous timing of PRF accurate pulse length and delay circuitry, a peak power sampling measurement capability based on an 80-nsec window and automatic phase shift control of the module. To assure proper control of RF input drive power to transceiver, a closed-loop sampling and leveling system was designed around the control computer. The resulting system is capable of leveling the input to within, typically, $\pm$ 0.1 dB. This modified SA equipment was used for all transmit mode measurements.

(U) All software for this pulse measuring system was developed at NRL and includes both measurement programs and data processing programs.

(U) Based on prior experience gained in making receiver measurements, it was evident that the amount of data to be stored as printed matter had to be further reduced and additionally that more rapid data measurement methods would be required to provide higher sampling rates than those used previously in making receiver measurements. By judicious choice of the order of measurement it was possible to reduce measurement time for a single data point to approximately 0.02 sec, including transfer of data to the computer. Thus measurements were made under

the following conditions and reported in Section 5:

a. 3 temperatures (-30°C, +20°C, +79°C)

b. 3 voltages (-2%, nominal, +2%)

c. 16 phase state (4 bits)

d. Frequency variation over band of interest

e. Measure peak power using single pulse and pulse averaging techniques vs Freq.

f. Measure insertion phase length vs Freq.

(U) The parameters measured are similar to an S parameter measurement of S_{21}. However, it was not practical to carry the error correction model to the same degree of accuracy employed in receive measurements due to overall system accuracy. It was found that for the test conditions encountered, and by the use of averaging techniques, that power could be measured to within $\pm$ 0.2 dB at a 75% confidence level and phase to within $\pm$ 1.5 degrees also with a high probability of success.

(U) As in the case of the receiver, transmitter data was placed on cassette magnetic tape for further processing.

(U) Processing, although quite thorough, resulted in summary data which was also placed on cassette magnetic tape. It was thus possible to further combine this processed summary data as dictated by visual inspection of the data. The following parameters were evaluated from the data stored on magnetic tape:

a. Power output;

b. Insertion phase;

1. error from linear vs freq.

2. error from quadradic vs freq.

3. RMS error all freq.

4. peak error from linear

c. Differential phase

1. max-min error vs freq.

2. overall max-min error

3. RMS error vs freq.

4. overall RMS error

(U) In addition to the detailed measurements described above a separate program was devised to measure peak power as a function of time through the pulse. The transceiver was operated in a standard pulse mode and the peak power was sampled throughout the pulse. This was accomplished by externally triggering the measurement cycle and synchronizing the trigger with the pulse envelope. The sampling window of the peak power meter is approximately 80 nsec so that peak instantaneous power based upon a part of a single pulse is possible. Plots of data accumulated in this manner are included in Section 5 of this report.

4.0 RECEIVER DATA

(U) Each transceiver module was evaluated under varying test conditions of temperature, voltage, and phase state. The data thus obtained, and summarized is included as Table I of this document.

(U) The following sections in conjunction with information from Table I are intended to give a detailed overview of each of the various important electrical parameters of the transceiver receiver channel.

4.1 RECEIVE INSERTION PHASE

(U) Insertion Phase is arbitrarily defined as the absolute phase length of the entire module receiver channel when the phase shifter is set to the zero phase state. The zero phase state is defined as the minimum or shortest phase length of a switched line type configuration.

(U) Insertion phase length, as a function of frequency, over the operating band, can be defined in terms of an equivalent length of air line plus an offset. This equivalency is based upon a best fit linear approximation to the data. However, to completely define insertion phase it is necessary to define both peak and RMS errors between this linear approximation and actual data. It is also possible to perform a best-fit operation assuming a curve based upon a higher order polynomial.

(U) Data recorded on each module is of such a form that, if desired, the following information can be generated.

A. Any phase state can be chosen as the reference state.

(U) TABLE I RECEIVER SUMMARY DATA‡

VENDOR	SERIAL NUMBER	TEMP*	VOLT*	ERROR IN Δ¢ PEAK	ERROR IN Δ¢ RMS	ERROR IN I¢ PEAK	ERROR IN I¢ RMS	VSWR MAX	GAIN AVG	GAIN RMS-SPREAD	GAIN DEVIATION	VARIATION IN AVG. GAIN $f_L \rightarrow f_H$	VARIATION IN GAIN DB f_L	VARIATION IN GAIN DB f_H	OFFSET IN AVG Δ¢ ERROR f_L	OFFSET IN AVG Δ¢ ERROR f_H	Δ¢ SPREAD AT ANY f
				DEG.	DEG.	DEG.	DEG.		DB	DB	DB	DB					DEG.
MA	2	L	L	4.95	1.88	1.95	1.01	1.23	33.3	.25	.94	0	±.25	±.25	0	+2	± 3
			N	5.09	1.92	1.97	1.02	1.23	33.6	.25	.95	0	±.25	±.25	0	+2	± 3
			H	4.98	1.88	2.0	1.02	1.23	33.7	.3	.96	0	±.25	±.25	0	0	± 3
		R	L	5.08	2.14	-2.18	1.00	1.25	32.6	.3	1.06	.25	±.25	±.25	+1	+2	± 3
			N	5.08	2.15	-2.12	.99	1.25	32.8	.3	1.04	.2	±.25	±.25	+1	+2	± 3
			H	5.05	2.17	-2.11	.99	1.25	32.9	.3	1.04	.2	±.25	±.25	+1.5	+1.5	± 3
		H	L	9.46	4.01	-11.83	4.89	1.25	30.6 MIN 32.4 MAX	--	2.86	1.8	±.25	±.8	-5	+5	± 6
			N	6.27	2.71	-12.07	4.96	1.26	30.7 MIN 32.9 MAX	--	2.93	2.2	±.25	±.3	+2	+2	± 3
			H	12.11	3.34	-6.91	2.43	1.26	31.1 MIN 32.8 MAX	--	2.66	1.7	±.25	±.25	--	8	± 3
MA	3	L	L	-4.49	1.68	2.69	1.06	1.36	32.8	.35	1.01	.25	±.2	±.2	-1	+1	± 3
			N	-4.69	1.73	2.62	1.06	1.37	32.95	.30	1.02	.2	±.3	±.3	-1	+1	± 3
			H	-4.56	1.71	2.60	1.07	1.36	33.1	.30	1.02	.2	±.25	±.25	-1	+1	± 3
		R	L	5.05	1.71	2.31	.98	1.33	31.8	.25	1.14	.3	±.3	±.3	0	+2	± 3
			N	4.93	1.70	2.31	.98	1.33	31.95	.35	1.15	.4	±.3	±.3	0	+2	± 3
			H	5.05	1.72	2.21	1.00	1.33	32.15	.3	1.14	.3	±.3	±.3	0	+2	± 3
		H	L	5.11	2.06	1.60	.85	1.35	30.1	.3	1.31	.4	±.3	±.3	+1	+2	± 2.5
			N	5.32	1.87	1.98	.90	1.35	30.2	.25	1.20	.4	±.25	±.25	0	+2	± 2.5
			H	5.05	2.07	1.59	.81	1.35	30.3	.3	1.18	.4	±.25	±.25	0	+2	± 2.5
MA	4	L	L	-4.77	1.84	-2.17	.98	1.39	33.3	.3	1.23	.3	±.25	±.25	-1	+1	± 4.0
			N	-4.81	1.86	-2.17	.98	1.39	33.5	.3	1.23	.25	±.25	±.25	-1	+1	± 4.0
			H	-4.76	1.83	-2.16	.97	1.39	33.65	.3	1.22	.4	±.30	±.30	-1	+1	± 4.0
		R	L	4.63	1.72	-2.08	.91	1.4	32.1	.3	1.37	.5	±.25	±.25	0	+2	± 3.5
			N	4.65	1.74	-2.16	.94	1.4	32.15	.35	1.40	.6	±.30	±.30	0	+2	± 3.0
			H	4.63	1.73	-2.09	.92	1.4	32.45	.35	1.36	.5	±.25	±.25	0	+2	± 3.5
		H	L	4.56	1.76	-5.01	1.76	1.25	30.3 MIN 31.5 MAX	--	2.02	1.2	±.25	±.25	0	+2	± 3
			N	4.85	1.85	-4.05	1.41	1.26	30.6 MIN 31.7 MAX	--	1.77	1.1	±.30	±.30	-1	+2	± 3
			H	4.99	2.29	-5.29	1.92	1.28	30.6 MIN 31.8 MAX	--	1.96	1.2	±.30	±.30	0	+2	± 2
MA	5	L	L	-5.07	1.68	1.86	.87	1.53	32.9	.3	1.13	.25	±.25	±.25	-1	+1	± 3.5
			N	-4.98	1.68	1.86	.87	1.53	33.05	.3	1.14	.25			-1	+1	± 4
			H	-5.29	1.68	1.93	.93	1.5	33.15	.3	1.10	.25			-1	+1	± 3.5
		R	L	4.70	1.86	1.90	.99	1.48	31.95	.3	1.12	0			0	+2	± 3.5
			N	4.56	1.82	1.94	1.00	1.48	32.15	.3	1.12				0	+2	± 3.5
			H	4.65	1.84	1.93	1.00	1.48	32.35	.3	1.16				0	+2	± 3.5
		H	L	4.94	2.14	1.87	.88	1.44	30.3	.25	.98				+1	+2	± 3
			N	4.81	2.11	1.84	.86	1.44	30.5	.25	1.00				+1	+3	± 3
			H	4.83	2.18	1.92	.91	1.44	30.7	.25	1.03	0	±.25	±.25	+1	+3	± 3
MA	6	L	L	4.26	1.51	-1.93	.88	1.38	33.25	.25	1.13	.5	±.15	±.15	-.5	+.5	± 2.5
			N	4.28	1.53	-1.97	.88	1.38	33.45	.25	1.12	.5	±.15	±.15	-.5	+.5	± 2.5
			H	4.46	1.57	-2.05	.92	1.38	33.55	.25	1.11	.5	±.2	±.2	0	+1	± 3
		R	L	5.16	1.80	-1.94	.83	1.33	32.4	.3	1.30	.5	±.25	±.25	0	+2	± 2.5
			N	5.17	1.82	-1.84	.81	1.33	32.7	.3	1.27	.5	±.25	±.25	0	+2	± 2.5
			H	5.13	1.88	-1.81	.80	1.33	32.7	.3	1.28	.5	±.25	±.25	0	+2	± 2.5
		H	L	UNIT FAILED DURING TEST													
			N														
			H														

(U) TABLE I RECEIVER SUMMARY DATA

VENDOR	SERIAL NUMBER	TEMP*	VOLT*	ERROR IN Δφ PEAK	ERROR IN Δφ RMS	ERROR IN Iφ PEAK	ERROR IN Iφ RMS	VSWR MAX	GAIN AVG.	GAIN RMS-SPREAD	GAIN DEVIATION	VARIATION IN AVG. GAIN $f_L \rightarrow f_H$	VARIATION IN GAIN DB f_L	VARIATION IN GAIN DB f_H	OFFSET IN AVG ERROR Δφ f_L	OFFSET IN AVG ERROR Δφ f_H	Δφ SPREAD AT ANY f
				DEG.	DEG.	DEG.	DEG.		DB	DB	DB	DB					DEG
RCA	1	L	L	UNIT FAILED DURING TEST													
			N														
			H														
		R	L	-7.32	2.44	2.44	.88	1.14	30.5	.35	1.57	.6	±.3	±.25	+3	-3	±3.5
			N	-6.75	2.41	2.53	.88	1.14	30.5	.25	1.32	.6	±.3	±.25	+2	-3	±3.5
			H	-6.68	2.34	2.58	.88	1.135	30.5	.30	1.42	.6	±.4	±.3	+1	-3	±3.5
		H	L	UNIT FAILED DURING TEST													
			N														
			H														
RCA	2	L	L	DATA NOT AVAILABLE													
			N														
			H														
		R	L	-9.66	4.43	1.87	.77	1.24	29.35	.35	1.35	.5	±.4	±.2	-1	-5	±4
			N	-9.52	4.38	1.91	.79	1.24	29.5	.35	1.33	.5	±.4	±.15	-1	-5	±4
			H	-9.60	4.50	1.91	.79	1.24	29.6	.4	1.36	.5	±.45	±.15	-1	-5	±4
		H	L	-8.06	3.86	-1.24	.46	1.22	27.4	.3	1.25	.3	±.5	±.2	-2.5	-4	±4
			N	-7.47	3.43	-1.24	.45	1.22	27.5	.3	1.12	.4	±.45	±.25	-2	-4	±4
			H	-7.65	3.65	-1.24	.46	1.22	27.6	.3	1.16	.4	±.4	±.25	-2	-4	±4
RCA	3	L	L	4.38	1.61	-2.83	1.10	1.36	31.0	.5	1.94	1.25	±.3	±.3	+2	-1	±2.5
			N	5.13	2.10	-2.82	1.14	1.36	31.1	.5	1.94	1.25	±.25	±.25	+2	0	±2.5
			H	4.31	1.55	-2.80	1.10	1.36	31.1	.5	1.97	1.25	±.25	±.25	+2	-1	±2
		R	L	4.97	1.80	2.50	.96	1.24	30.1	.25	1.29	.6	±.4	±.25	+3.5	0	±2
			N	5.28	1.98	2.57	.96	1.24	30.2	.25	1.26	.6	±.4	±.2	+3.5	0	±2
			H	5.57	2.05	2.52	.95	1.24	30.3	.2	1.26	.6	±.4	±.25	+3	0	±2
		H	L	5.21	2.42	-1.53	.50	1.325	27.7	.1	.89	.1	±.4	±.2	+2	+2	±2
			N	5.17	2.42	-1.67	.54	1.325	27.9	.15	.91	.2	±.4	±.25	+2	+2	±2
			H	5.90	2.88	-1.69	.55	1.325	28.1	.15	.89	.3	±.35	±.25	+3	+3	±2.5
RCA	4	L	L	DATA NOT AVAILABLE													
			N														
			H														
		R	L	-8.47	4.54	1.65	.94	1.22	29.4	.25	1.48	-.35	±6	±.35	-3	-4	±4
			N	-8.73	4.68	1.62	.93	1.22	29.55	.25	1.48	-.25	±.65	±.35	-3	-4	±4
			H	-8.47	4.42	1.59	.90	1.22	29.65	.25	1.46	-.25	±.6	±.4	-3	-4	±4
		H	L	-5.81	3.19	-1.18	.66	1.24	26.75	.35	1.59	-.35	±.9	±.5	-3	-3	±3
			N	-5.86	3.19	-1.04	.61	1.24	26.85	.35	1.58	-.25	±.65	±.5	-3	-3	±3
			H	-6.06	3.35	1.41	.77	1.23	27.0	.35	1.59	-.30	±.65	±.5	-2	-3	±3
RCA	5	L	L	6.49	1.54	-1.36	.60	1.48	30.0	.5	2.07	1.0	±.5	±.4	+3	-2	±3
			N	-6.71	2.72	-1.29	.57	1.48	30.1	.55	2.12	.75	±.7	±.6	0	-3	±4
			H	-6.40	2.29	-1.19	.53	1.48	30.1	.45	2.04	1.0	±.6	±.45	+2	-4	±3
		R	L	-7.22	2.51	2.17	.77	1.33	29.45	.4	1.67	.75	±.6	±.25	0	-5	±3
			N	-7.07	2.37	2.25	.80	1.33	29.6	.4	1.70	.7	±.6	±.35	0	-4	±3
			H	-7.29	2.55	2.23	.78	1.33	29.75	.4	1.73	.5	±.6	±.35	0	-5	±3
		H	L	-4.73	1.56	.89	.50	1.24	27.1	.30	1.28	0	±.6	±.3	+1.5	-2	±3
			N	-6.14	2.32	-1.03	.52	1.24	27.4	.35	1.55	0	±.7	±.45	0	-3	±3
			H	5.78	1.54	- .91	.49	1.24	27.65	.35	1.27	0	±.3	±.3	+3	-2	±3

Table continues

(U) TABLE I (CONCLUDED - RECEIVER SUMMARY DATA‡

VENDOR	SERIAL NUMBER	TEMP*	VOLT*	ERROR IN Δφ PEAK	ERROR IN Δφ RMS	ERROR IN Iφ PEAK	ERROR IN Iφ RMS	VSWR MAX	GAIN AVG.	GAIN RMS-SPREAD	GAIN DEVIATION	VARIATION IN AVG. GAIN $f_L \rightarrow f_H$	VARIATION IN GAIN DB f_L	VARIATION IN GAIN DB f_H	OFFSET IN AVG Δ‡ ERROR f_L	OFFSET IN AVG Δ‡ ERROR f_H	Δ‡ SPREAD AT ANY f
				DEG.	DEG.	DEG.	DEG.		DB	DB	DB	DB					DEG.
RCA	6	L	L	DATA NOT AVAILABLE													
			N														
			H														
		R	L	>12	--	-1.61	.78	1.25	30.55	.55	1.82	.25			--	--	--
			N	>12	--	-1.57	.74	1.25	30.6	.55	1.83	0	±.85	±.35	--	--	--
			H	>12	--	-1.52	.75	1.25	30.7	.5	2.0	0	±.85	±.35	--	--	--
		H	L	-9.20	5.42	1.34	.53	1.225	28.5	.35	1.66	-.25	±.8	±.4	-1	-6	±7
			N	-9.08	5.42	1.32	.51	1.225	28.7	.3	1.67	-.25	±.8	±.35	-1	-6	±7.5
			H	-9.21	5.49	1.37	.52	1.225	28.8	.4	1.65	-.25	±.8	±.3	+2	-6	±7

*TEMP: L = -30°C R = +20°C H = +70°C

*VOLT: L = -2% N = NOMINAL H = +2% (ALL VOLTAGES SET TO L, N, OR H)

‡SEE TEST FOR FURTHER DESCRIPTION OF DATA

B. The best-fit approximation can be defined by any curve desired if an appropriate algorithm can be written. The errors can be defined in terms of peak, average or RMS, on a single frequency basis or aggregate over all frequencies of interest.

C. The data can be analyzed in terms of operating or instantaneous band parameters as deemed necessary by the system analyst.

(U) For the purpose of this evaluation the data was reduced in terms of a best-fit linear and quadratic approximation over the full operating band. In addition, a linearity calculation was made over the instantaneous band of interest. This band was stepped through the operating band in increments equivalent to the measurement frequency increments (5 MHz).

(U) Referring to Table I, it was found based upon a best-fit, operating-band, linear approximation, that an error of $\pm$ 10 degrees is realizable and can probably be reduced to $\pm$ 5 degrees depending upon system demand. Based upon instantaneous band data, a peak error of less than $\pm$ 5 degrees is definitely practical. However it should be noted that from the error slope; $\frac{\phi E}{\Delta f}$, the ratio of the error (deviation from the ideal straight line) to the frequency typically exceeds .7 degrees/MHz. Some of this deviation is undoubtedly a result of measurement accuracy but if carried to its limit (assuming no measurement system inaccuracy) might still present a problem for high doppler resolution system with more stringent phase-vs-frequency requirements.

(U) It is concluded, from the recorded data, that modules can be manufactured where the following parameters are met:

a. Single module basis - (where absolute insertion phase length is not critical)

   1. Over the operating band the insertion phase deviation from linear best fit to the data less than $\pm$ 5 degrees; RMS error, all frequencies, 2 degrees.

b. Multiple unit basis (where unit to unit phase equivalence is important):

   1. Compared to reference linear phase length:

      peak error $\pm$ 15 degrees;

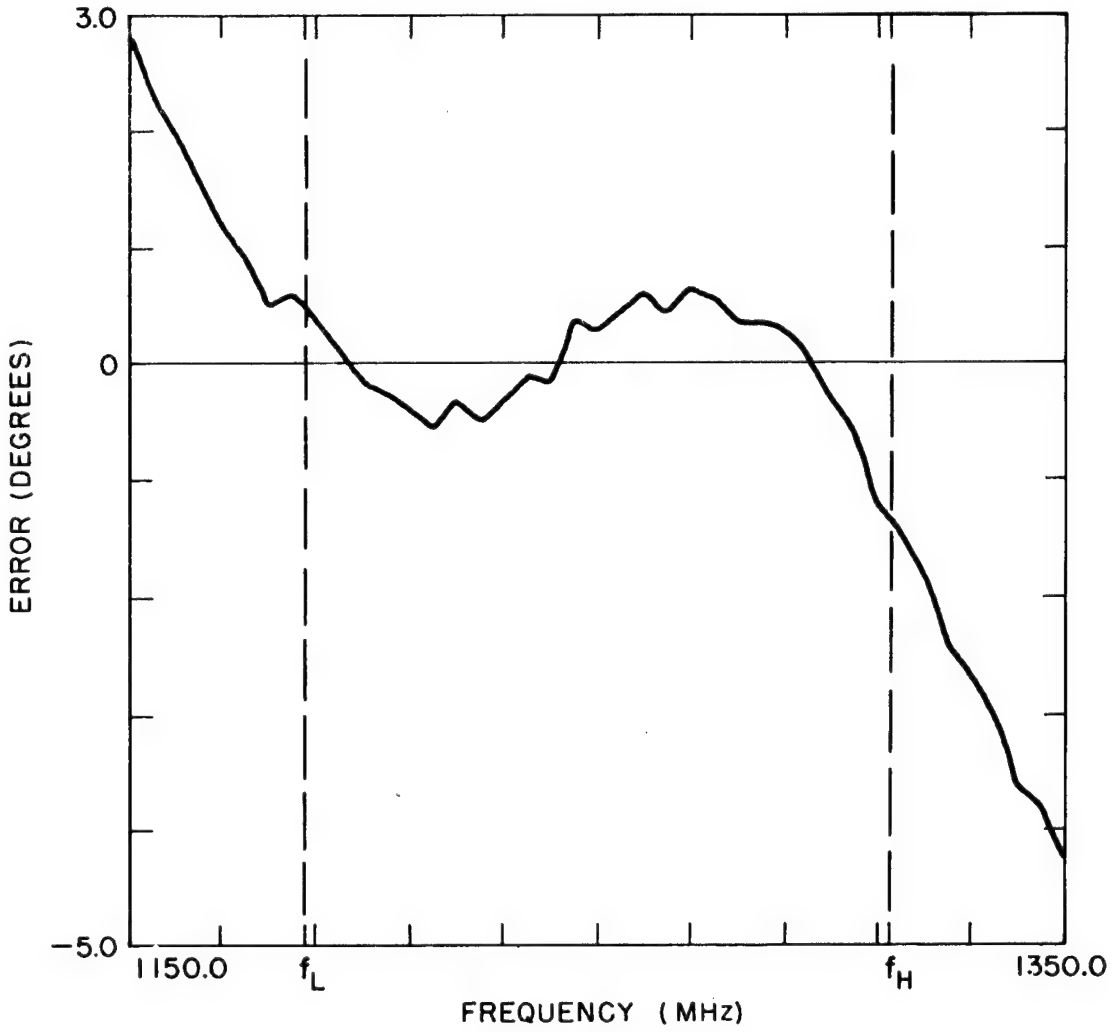
      RMS error at f_{center} = 5 deg, band edges = 7 deg.

c. All higher order perturbations whether in terms of operating or instantaneous band parameters should be referenced back to an operating band linear phase characteristic to assure a practical working reference for manufacturing.

Figure 7 is a plot of insertion phase error vs frequency. Data on this RCA unit is an example of one of the test conditions reported in Table I. Similar data for all test conditions was obtained. In addition, the maximum peak value (anywhere in the operating band) and the RMS va lue (over the operating band) from linear are recorded in Table I and are good indicators of the overall insertion phase performance of the units evaluated.

MODULE ID: RCA2
TAPE ID: MBL 112
FILE ID: RCA2 6/20/74 HHO
FILE NO: 33 REF. FILE: 33

PROC. DATE: JUNE 24,1974
DATA DATE: JUNE 20,1974
TEMP: HIGH (+70°C)
VOLT: HIGH (+2%)



(S) Fig. 7 - Insertion phase error (from linear approximation vs frequency)

(U) 4.1.1 RCA DATA - from the data of Table I all RCA modules performed in a manner that is probably acceptable for most phased-array applications. Linearity was quite good; however, questions are raised when this data is coupled with some rather large measured differential phase errors. Is the reference phase state "0" stable and acceptable resulting in many other phase states being of questionable performance quality, or is bit "0", the reference state, the offender?

(U) The answer can only be obtained through additional thorough analysis of internal circuits of the modules to result in a better understanding of the causes of the noted differential phase errors. Based upon the assumption that phase state 0 is defined as insertion phase or reference state, the RCA data is well within acceptable limits.

(U) 4.1.2 MA DATA - As was the case with the RCA modules, the insertion phase data (based upon bit 0 as the reference state) is acceptable. The errors recorded were greater than those observed on the RCA modules but due to measurement system noise that existed during the evaluation of the MA modules, this apparent increase in error over the RCA data may not be factual. Measurements were not repeated since the data was considered to be well within acceptable limits with indication of adequate insertion phase control during manufacture.

(U) The MA modules experienced performance difficulty at the maximum operating temperature. Insertion phase error of two of 5 modules increased drastically while one module performance was considered unacceptable. It appears that this is an indirect error in that the cause is associated with some form of detuning over the frequency band.

Detuning is evidenced in the large deviations in gain as a function of frequency noted for these particular test conditions. Further design effort to improve stability at high temperature is definitely indicated.

4.2 DIFFERENTIAL PHASE DATA

(U) Differential phase is defined as the difference in insertion phase between any commanded phase state and the reference (bit 0) state. Because switched line lengths are used, the resultant differential phase is designed to be exactly the nominal value at only one frequency. This frequency is determined by system parameters and is adjustable during the design phase of the module.

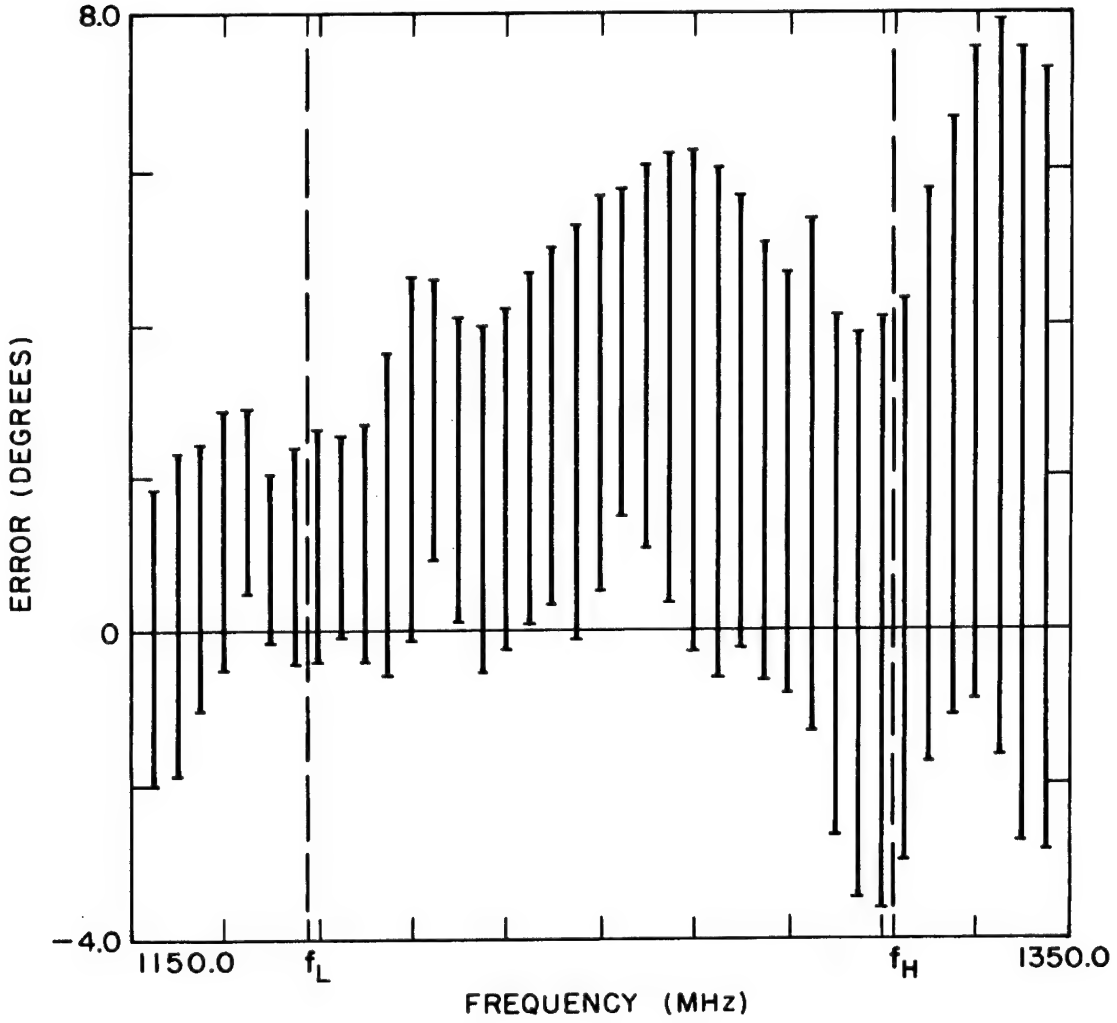
(U) Since any deviation from the design value is considered an error, it is possible to generate a truly random error about some mean error value plus errors that reflect an average bias or mean that is not zero from the design value. In addition, the magnitude of both types of errors can be frequency dependent but independent of each other.

(U) Because of the various types and dependency relationships possible, errors in Table I have been described as RMS (over operating band referenced to desired value, not mean error), peak error (at any frequency or phase state), and bias (offset) or systematic error with frequency. Also general information about peak to peak error with phase state at any frequency is given. This data is derived from curves similar to those seen in Figures 8a and 8b.

(U) Of all the units evaluated, those supplied by MA were consistently closer to the desired values. For the MA units, RMS errors were in

MODULE ID: MA2
TAPE ID: MBL 105
FILE ID: MA2 6/11/74 HHO
FILE NO: 0 REF. FILE: 17

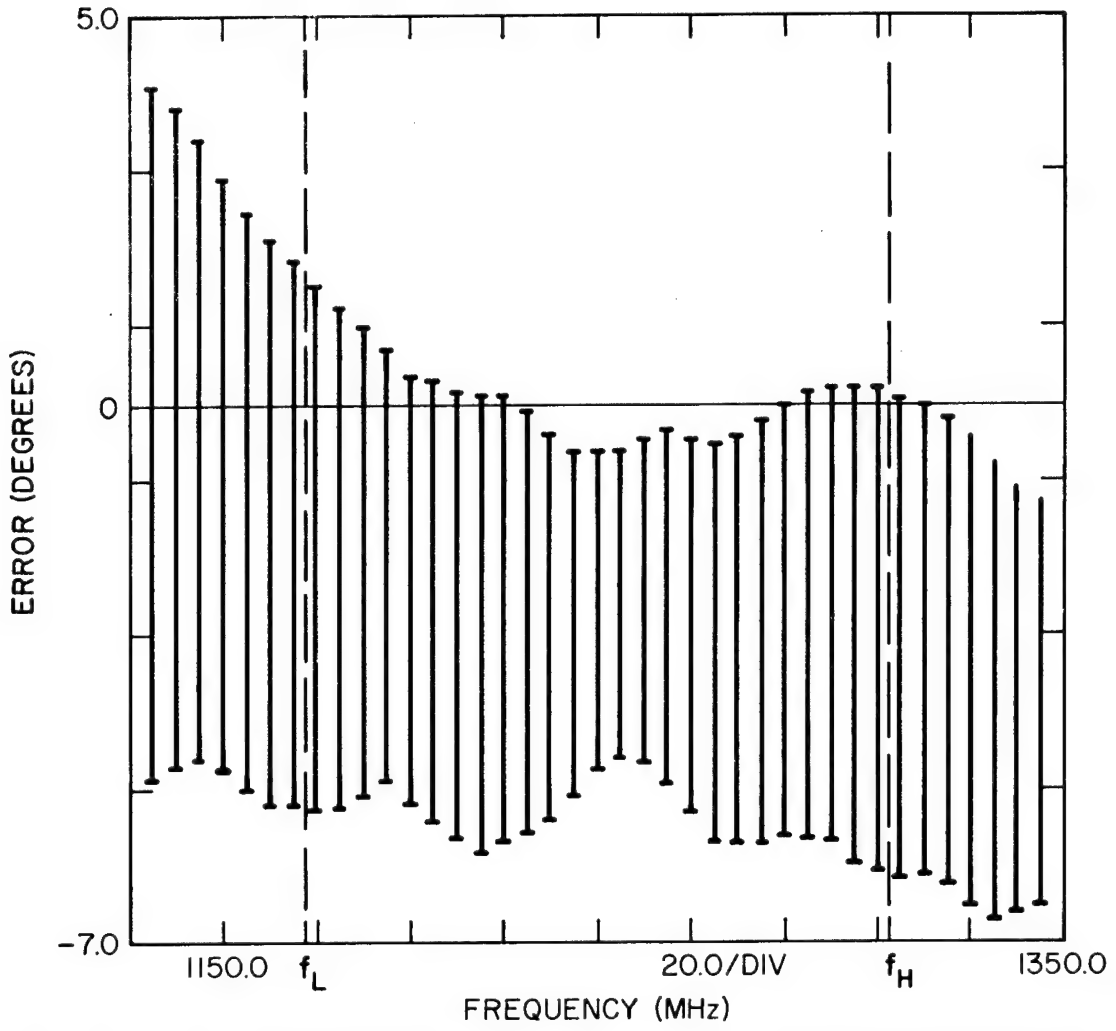
PROC. DATE: JUNE 11, 1974
DATA DATE: JUNE 11, 1974
TEMP: HIGH (+70°C)
VOLT: NORMAL



(S) Fig. 8a - Differential phase error spread vs frequency
(Microwave Associates #2)

MODULE ID: RCA4
TAPE ID: MBL 111
FILE ID: RCA4 6/20/74 HHO
FILE NO: 0 REF. FILE: 1

PROC. DATE: JUNE 24, 1974
DATA DATE: JUNE 20, 1974
TEMP: HIGH (+70°C)
VOLT: HIGH (+2%)



(S) Fig. 8b - Differential phase error spread vs frequency (RCA #4)

general lowest at cold (-30°C) temperatures, the errors increasing with temperature. Since the RMS error is referenced in Table I from the nominal or desired value, it includes any bias or offset that isn't random. This bias is also recorded separately in Table I under the column heading "OFFSET IN AVG. $\Delta\phi$ ERROR". This bias appears to be frequency and temperature dependent. The temperature dependency is reasonable in that differential phase increases with temperature; explainable by expanding lines. It is however difficult to explain or justify errors associated with frequency without knowledge of internal modules details. If this bias were eliminated, then RMS and peak errors would certainly be reduced; but the recorded values appear to be quite adequate to meet typical system requirements.

(U) Some degradation was noted on MA modules at high (+70°C) temperature. This degradation appears to be related to gain/frequency distortion and indicates further development prior to further procurement for a specific system application.

(U) All RCA units were not evaluated at low (-30°C) temperature. One unit (Ser. #6) showed errors greater than 1/2 the least significant bit (LSB = 22.5°) such that the computer evaluation program could not properly determine the bit called. Much of this error appeared to be a bias from the design value.

(U) In addition, on RCA units, it was repeatedly found that the differential phase-frequency response was appreciably different from the desired values for the small bits (22.5°, 45°, 67.5°). Although peak deviations were small (less than 10°), percentage-wise, errors of [illegible] from desired were noted.

(U) Again it is impossible to properly ascertain the cause of this error without a thorough study of the basic module internal circuit details. It is reasonable to confidently predict phase shifter designs that can yield (in production) peak errors less than $\pm 5^{o}$ with RMS errors of 2.5^{o} and with maximum bias offset at any frequency, temperature, and voltage less than $\pm 2.0^{o}$.

4.3 DIFFERENTIAL PHASE STATE CONTROL

(U) Each module developer selected a logic control design based upon best estimates (their own) of present and future system criteria. Individual logic configuration was then incorporated into module design and as such must be considered as part of overall quality just as the direct microwave path circuitry. It has become obvious that primary design and development efforts were directed towards the RF circuitry to the extent that much less attention was directed to logic circuit design.

(U) MA employed TTL logic chips in a special hybrid package, whereas RCA chose to make use of CMOS* chips. Each has certain advantages and final choice will be dictated by the system application. However, experience on this program has produced some insights not previously recognized:

A. The chosen module logic design should include only those features necessary to accomplish the desired system function. The addition of universal features to increase compatibility

*Complementary metalization on silicon; RCA trademark.

with multiple applications has rapidly resulted in designs that are not truly reliable nor ideal to any specific application.

B. The logic design must have fail-safe turn-on capability. It should not be necessary to turn on dc power in any special sequence. If for any reason such turn on sequencing is indicated (such as the restriction of CMOS logic to voltages applied to signal lines without prior application VCC) proper precautions should be built into the logic to prevent damage while meeting all other logic requirements (such as speed, impedance, current, etc).

C. The design should permit 100% of the time operation either in transmit or receive mode. This does not mean 100% rf duty factor in the transmit mode but rather to negate any requirement to continuously cycle between transmit and receive.

D. The design should be inherently fail safe. This condition should prevail at all temperatures including those beyond normal operating limits.

E. Full burn-in of all logic (including bias control logic), should be incorporated even for limited quantity experimental units unless the logic is easily removable from the module.

4.4 RECEIVE VSWR

(U) In array applications it is difficult to assess the importance of peak VSWR of one module at a single frequency. Even though this magnitude has little direct application to system performance, it is an indicator of module quality and stability.

(U) Both MA and RCA had VSWR maxima that are beyond original guideline specifications. Even though both contractors encountered difficulty in obtaining adequate match, it is believed to be within the limits of present state of the art to obtain better performance than that demonstrated. Based upon peak value alone, no statistical trend with temperature or voltage is noted.

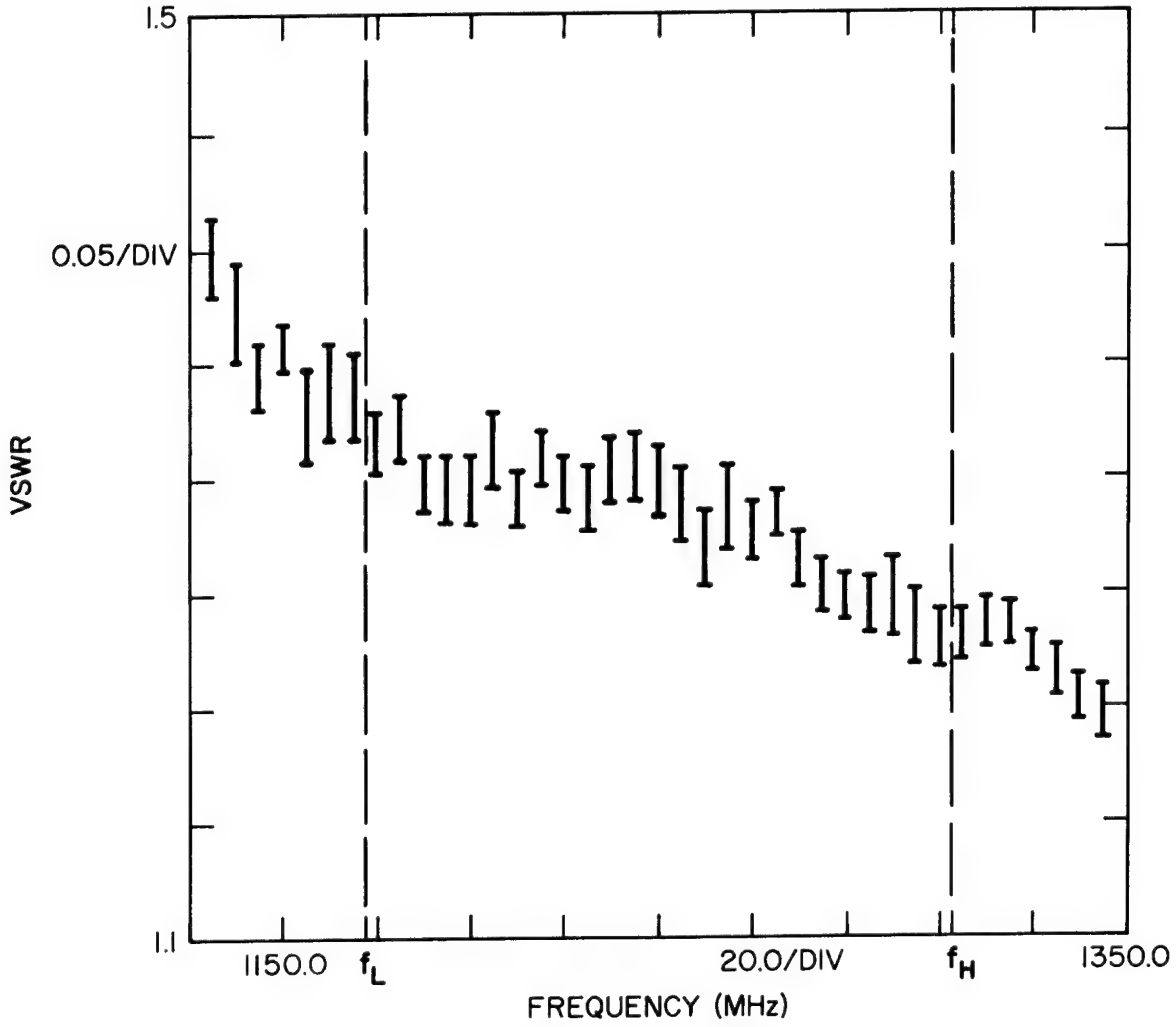
(U) It has been observed from data similar to Figures 9A and 9B that the spread in VSWR at each frequency over all phase states and the average overall frequencies is greater for MA modules than RCA units. Several fundamental reasons can be given for this performance, most of which without a thorough analysis of design details, are simply conjecture. However one speculation that appears valid is related to the trade-off in design between input VSWR and receiver noise figure. (See Section 4.6) It should be practical to design for VSWR maxima (under all conditions of temperature, phase state, and voltage) of less than 1.3 with an anticipated production design average of 1.25 considered reasonable.

4.5 RECEIVE GAIN

(U) Unlike transmitter performance, where minimum power is the criterion,

MODULE ID: MA3
TAPE ID: MBL 103
FILE ID: MA3 6/10/74 RNO
FILE NO: 0 REF. FILE: 17

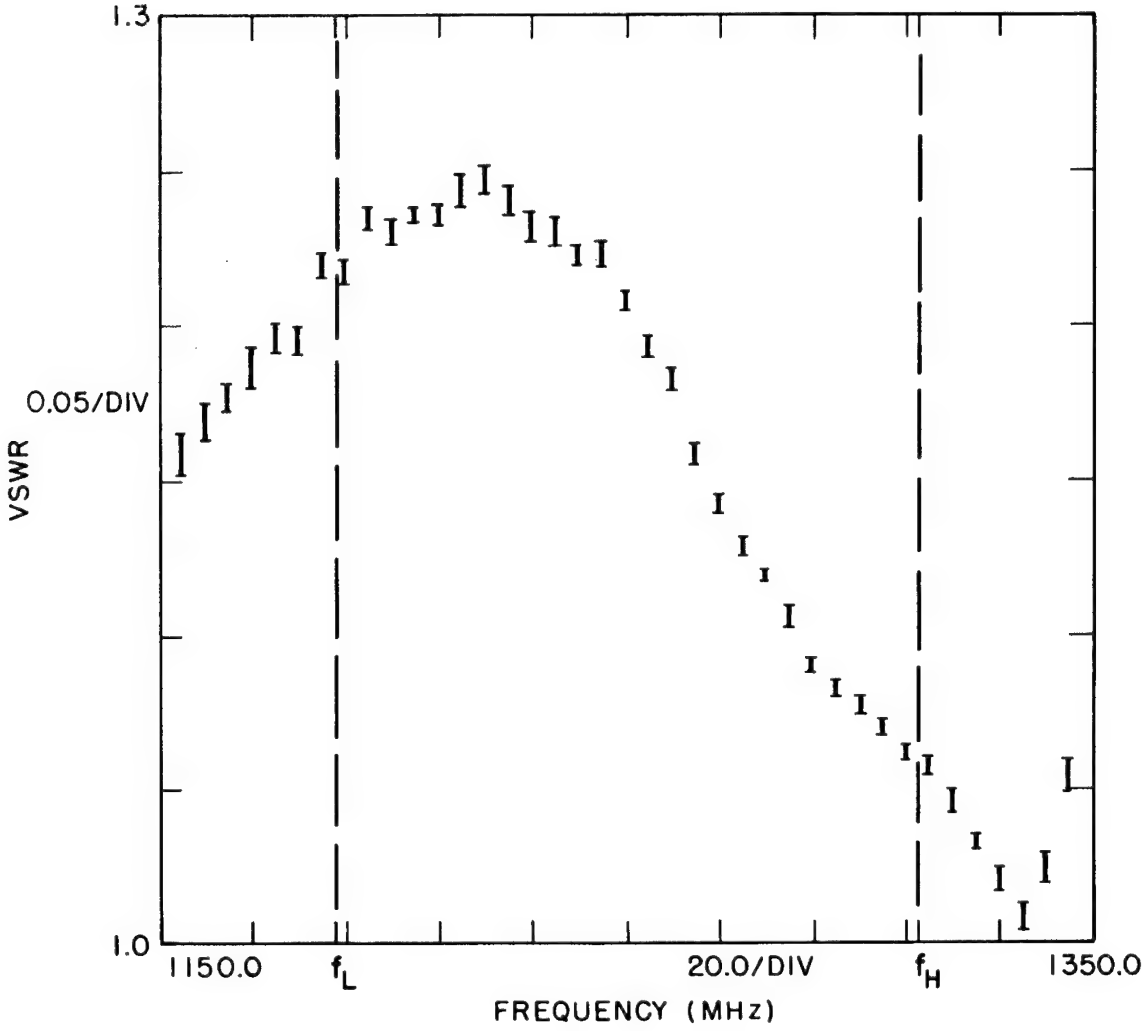
PROC. DATE: JUNE 11, 1974
DATA DATE: JUNE 10, 1974
TEMP: ROOM (+20°C)
VOLT: NORMAL



(S) Fig. 9a - VSWR spread vs frequency (Microwave Associates #3)

MODULE ID: RCA6
TAPE ID: MBL 110
FILE ID: RCA6 6/17/74 RLO
FILE NO: 0 REF. FILE: 33

PROC. DATE: JUNE 18, 1974
DATA DATE: JUNE 17, 1974
TEMP: ROOM (+20°C)
VOLT: LOW (−2%)



(S) Fig. 9b -VSWR spread vs frequency (RCA #6)

the receiver portion of the module is specified in terms of gain. Curves such as Figure 10A and 10B have been obtained and are included to illustrate maximum and minimum module gain at each frequency for specific test conditions of temperature and voltage.

(U) If these modules are intended for array applications, such parameters as instantaneous variation in gain over the array (rather than for a single unit) are of importance. If the module evaluated is considered typical of all modules, then the spread in gain with phase state can be translated to instantaneous array spread. Likewise, for array bandwidth purposes, average values of gain (averaged over all phase states at each frequency) appear to be a more meaningful indication of instantaneous performance at each phase state.

(U) For these reasons Table I lists several gain parameters:

A. Average Gain - in dB this is the average of measured gain over frequency and phase state for specific test conditions relative to temperature and voltage.

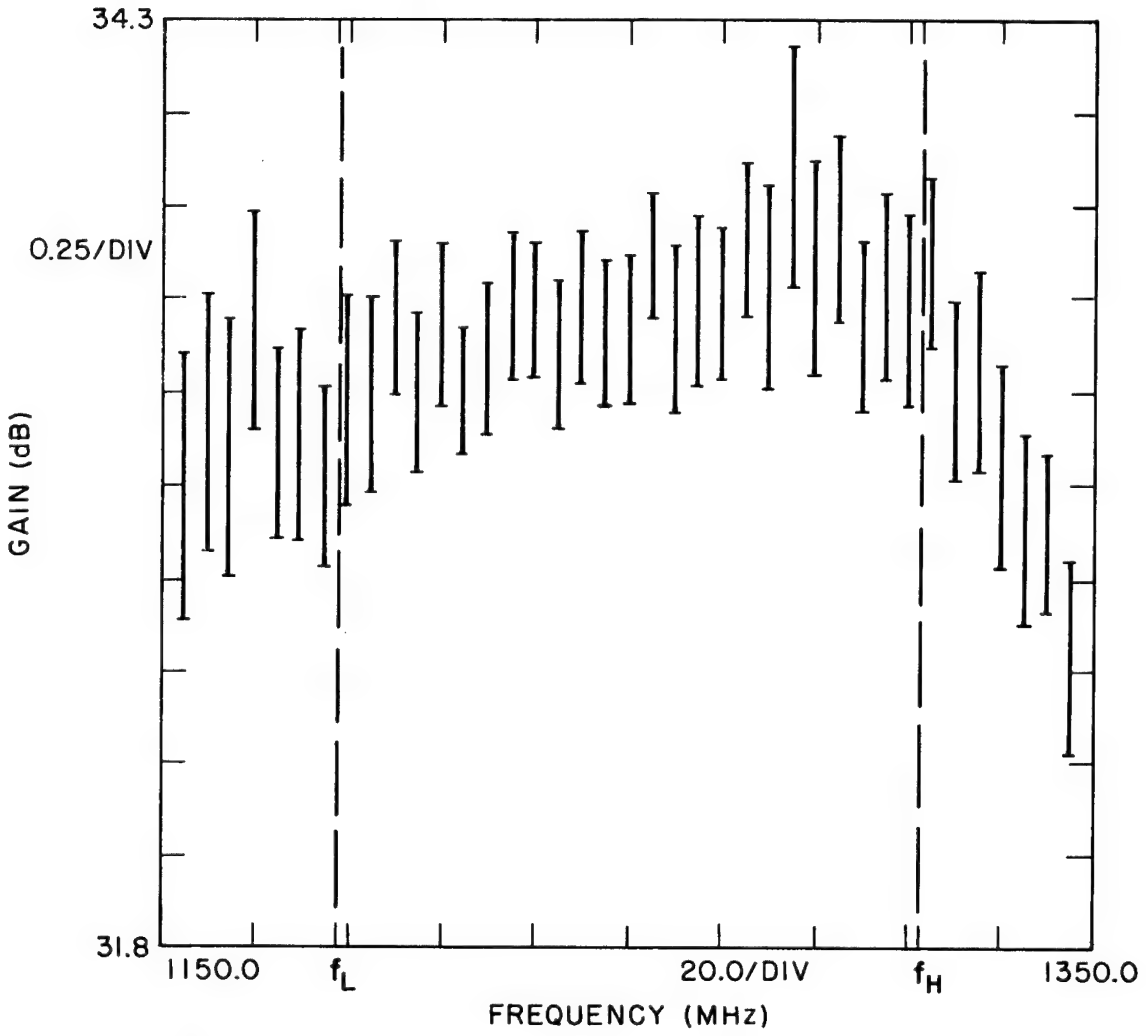
B. RMS Gain - in dB this value specifies the spread in Gain about the average value, and includes effects with frequency.

C. Gain Deviation - this is the peak to peak gain variation for the test conditions of temperature and voltage at any frequency and phase state. In array applications this value would be representative of the type of variations that might be expected over an array; however the RMS value has more statistical meaning.

D. Data relating to frequency response of the average gain

MODULE ID: MA4
TAPE ID: MBL 100
FILE ID: MA4 6/6/74 LNO
FILE NO: 0 REF. FILE: 17

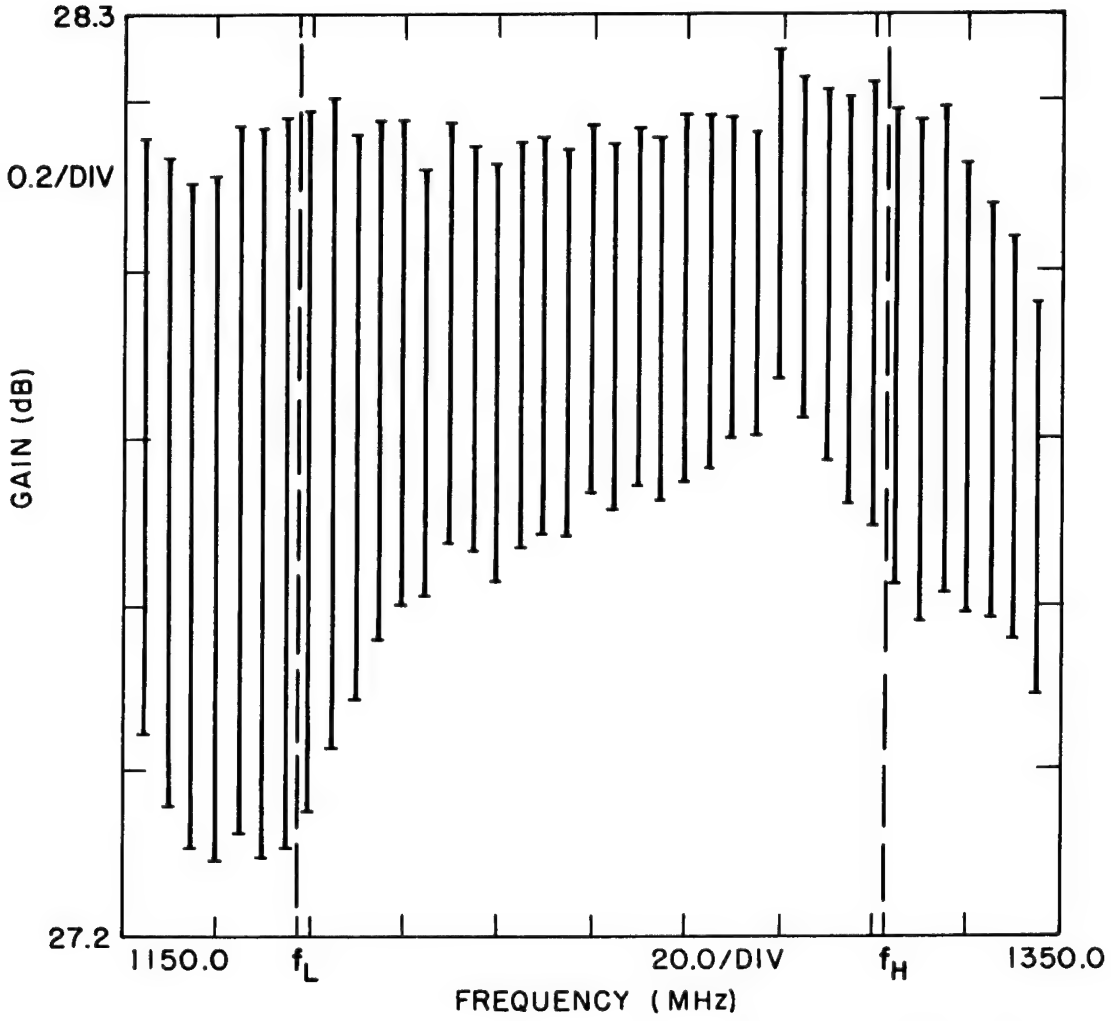
PROC. DATE: JUNE 7, 1974
DATA DATE: JUNE 6, 1974
TEMP: LOW (−30°C)
VOLT: NORMAL



(S) Fig. 10a - Receiver gain spread vs frequency
(Microwave Associates #4)

MODULE ID: RCA3
TAPE ID: MBL 113
FILE ID: RCA3 6/20/74 HNO
FILE NO: 0 REF. FILE: 17

PROC. DATE: JUNE 24, 1974
DATA DATE: JUNE 20, 1974
TEMP: HIGH (+70°C)
VOLT: NORMAL



(S) Fig. 10b - Receiver gain spread vs frequency (RCA #3)

(averaged over phase states) and maximum peak to peak gain at any single frequency is indicated.

(U) 4.5.1 RCA DESIGN PERFORMANCE - The average gain slope over frequency varied sufficiently unit to unit such that no trend could be established. Some units exhibited increases in gain with frequency, while others exhibited definite decreases. It is noted that the variation was most prominent at cold ($-30^{o}C$) temperatures, reaching a magnitude as great as 1.25 dB. At high ($+70^{o}C$) temperatures, the largest variation noted was .45 dB.

(U) This intrinsic slope in the average gain (averaged over all phase states) resulted in peak-to-peak (at any frequency and phase state) gain variations as great as 2.12 dB, with an average value of 1.52 dB over all temperatures and voltages. This peak-to-peak gain variation and the RMS gain variation over all frequencies was greater than that noted on the MA units.

(U) A gain variation also was noted with both temperature and DC supply voltage.

(U) Over the variation in supply voltage of +2% to -2% about nominal, the power gain did not change as would be predicted. This indicates some internal voltage compensation and/or change in efficiency. In addition it was found that at $-30^{o}C$ the change in output power averaged only .1 dB for 4% change in voltage whereas it increased to .34 dB at $+ 70^{o}C$.

(U) The existence of these non-uniform module performance characteristics, if repeatable (as was the case with the units evaluated), over all

production units would not be considered objectionable and would permit a relaxation in DC voltage control at cold temperatures.

(U) All units exhibited a decrease in gain with increasing temperature, and as with the MA modules, the response was found to be non-linear over the 100°C operating temperature range. A change of -0.01 dB/°C was noted from -30°C to +20°C and -0.0317 dB/°C from +20°C to +70°C.

(U) Overall receive gain, under all test conditions, exceeded the specification value of 25 dB. At room temperature (+20°C), nominal DC voltage, the unit to unit gain varied between 29.5 dB and 30.6 dB.

(U) 4.5.2 MA DESIGN PERFORMANCE - Except for high (+70°C) temperature performance on two units, the MA modules exhibited variation in the average gain with frequency from flat to a maximum of 0.6 dB. At any single frequency the peak-to-peak variation was typically 0.5 dB (± 0.25 dB about avg.). The two units that failed under high temperature operation exhibited a collapse in the frequency performance. The cause of the sudden collapse and likewise, the recovery when temperatures were again reduced, is presently unknown.

(U) RMS spread in gain about the average (averaged for all frequencies) was seen to be typically 0.3 dB with gain very uniform for all test conditions.

(U) Average gain (averaged over all frequencies and phase states) showed a sensitivity to voltage and temperature. With voltage, over the limits of +2% to -2% variation about nominal value the modules exhibited a typical sensitivity of 0.325 dB at all temperatures.

(U) The power-gain variation as a function of temperature (maintaining a constant DC input voltage) was found to vary over the units evaluated. In all cases, gain decreased with increase in temperature and the response was non-linear. Averaging the data of Table I over all the units, the drop in gain was 0.0137 dB/^{o}C from -30^{o}C to +20^{o}C and increased to 0.0243 dB/^{o}C from +20^{o}C to +70^{o}C.

(U) Overall receiver gain was, for all test conditions, in excess of the specification minimum of 25 dB. At room temperature (+20^{o}C) nominal DC voltage, the unit to unit gain varied from a minimum of 31.95 dB to a maximum of 32.8 dB.

4.6 RECEIVE NOISE FIGURE AND GAIN COMPRESSION

(U) The transceiver modules were evaluated for receiver noise figure and receiver compression.

(U) Noise figure was calculated on the basis of input to the module, not input to the first stage of amplification and as such includes circuit and the ferrite circulator losses.

(U) Compression was defined as that input power at which the receiver gain was 1 dB below that measured at low signal levels. Table II is a tabulation of noise figure as a function of frequency for the various modules evaluated. Included as part of this table are the input power levels at which compression occurred.

(U) In general the 1-dB compression point was noted at a higher input power level for RCA units than MA units; however, compression was more gradual on the RCA units with compression starting at approximately

(U)TABLE II-NOISE FIGURE AND GAIN COMPRESSION

a. NOISE FIGURE - dB

MODULE #	FREQUENCY								
	f-70	f-50	f-30	f-10	f_c	f+10	f+30	f+50	f+70
MA-2	2.93	2.99	2.93	3.03	2.96	2.96	2.96	3.11	3.14
MA-3	3.03	2.96	3.03	3.03	3.03	2.96	2.99	3.01	2.89
MA-4	2.85	2.96	2.96	3.03	2.94	2.96	2.89	2.96	3.03
MA-5	3.03	3.11	2.84	3.18	3.11	3.18	3.18	3.26	3.11
MA-6	UNIT FAILED PRIOR TO N.F. MEASUREMENT								
RCA-1	UNIT FAILED PRIOR TO N.F. MEASUREMENT								
RCA-2	3.41	3.41	3.33	3.33	3.18	3.11	3.26	3.30	3.26
RCA-3	MEASUREMENTS NOT AVAILABLE								
RCA-4	3.18	3.18	3.11	3.13	3.18	3.33	3.50	3.76	3.76
RCA-5	3.33	3.03	3.18	3.33	3.30	3.26	3.18	3.41	3.58
RCA-6	3.18	3.15	3.33	3.29	3.29	3.41	3.41	3.55	3.72

b. GAIN-COMPRESSION-DBM (FOR 1-dB COMPRESSION)

MODULE #	COMPRESSION-DBM	REMARKS
MA-2	-27.3	STARTS AT -29 DBM
MA-3	-27.9	- - - -
MA-4	-28.3	- - - -
MA-5	-27.8	- - - -
MA-6	UNIT FAILED PRIOR TO MEASUREMENT	
RCA-1	UNIT FAILED PRIOR TO MEASUREMENT	
RCA-2	-24.2	STARTS AT -27 DBM
RCA-3	MEASUREMENTS NOT AVAILABLE	
RCA-4	-24.2	STARTS AT -27 DBM
RCA-5	-25.9	STARTS AT -29 DBM
RCA-6	-25.0	STARTS AT -28 DBM

the same input power (typically -28 DBM) for all units.

(U) It is concluded that a 1-dB compression point of -25 DBM is not practical for present state of the art devices. It also appears from the data obtained, that good linearity (no compression) below -30 DBM is to be expected.

(U) The modules will typically operate for all input modes except those due to excessively large receive input signals and even then will not be permanently damaged, since burn-out requires powers much in excess of the compression level.

(U) No attempt was made to measure receiver recovery time after being subjected to large input signals.

4.7 RECEIVER ISOLATION

(U) Isolation can be used as a check of internal design integrity of the transceiver modules. It is a measure of the separation of the transmitter and receiver sections of the unit which, if not properly isolated, could result in resonances, oscillations, non-linearities, and possibly permanent damage.

(U) Receiver isolation is defined as the isolation between manifold port (as input) and antenna port (as output) with the transceiver in the receive mode and DC voltages applied.

(U) Under these conditions of test a typical device exhibited a minimum isolation of 45 dB and a maximum of 60 dB over the operating band. These values were well within the specification limits and should be sufficient to assure proper operation of the module in the two normal modes of operation.

5.0 TRANSMITTER DATA

(U) Each module or transceiver was evaluated under varying conditions of temperature, input drive, and power supply voltage, over all phase states, for transmit characteristics. The data thus obtained has been summarized and organized into Table III.

5.1 INSERTION PHASE

(U) Insertion phase has been defined as the effective electrical length of the microwave path through the module in degrees with the phase shifter set to minimum length or bit 0. For purposes of evaluation a best-fit straight line was derived ($\phi = Mf + B$) from the measured data over the operating band. Errors as a function of frequency were converted into RMS errors at each frequency and also a single value for all frequencies. The best-fit data was further analyzed to determine behavior with temperature, voltage and rf drive level. It should be noted that all differential phase data was referenced to the actual data of bit 0 for the specific conditions of test, not the best fit straight line. In this way it was possible to separate the variables of insertion and differential phase.

(U) No attempt was made to translate the actual data into higher order polynomials and to derive higher order insertion phase linearity terms; however, the data with temperature, voltage, and drive power indicates that for all instantaneous test conditions higher order terms (quadratic, etc.) are to be expected. Compared to best-fit

(U) TABLE III TRANSMIT DATA SUMMARY

VENDOR	SERIAL NUMBER	TEST CONDITIONS: TEMP.	VOLTAGE	INPUT POWER (DBM)	ERROR IN INSERTION PHASE: PEAK (DEG)	RMS (DEG)	ERROR IN DIFFERENTIAL PHASE (DEG): RMS (AVG)‡	RMS (MAX)‡	OUTPUT POWER (PEAK)‡: AVG. ALL FREQ.	RMS ABOUT AVG.	SPREAD IN AVG.	OVER ALL TEST CONDITIONS	REMARKS
MA	3	LOW	-2% to +2%	19,20,21	-4.8,+8	3.63	2.52	4.35	51.72DBM	.28DB	.6DB	51.5DBM	Δ¢ ERROR OFFSET TO 1.61 DEG
		ROOM	-2% to +2%	19,20,21	-3.6,+6.2	3.92	2.53	3.55	51.29DBM	.23DB	.5DB	.34 DBM RMS .6 DBM SPREAD	Δ¢ ERROR OFFSET TO 1.89 DEG
		HIGH	UNIT FAILED AT ≈ 40°C NO DATA AVAILABLE										
MA	4	LOW	-2% to +2%	19,20,21	----	----	----	----	51.72DBM	.36DB	1.0DB		PHASE COMMANDS ERATIC
		ROOM	-2% to +2%	19,20,21	-9,+5	3.29	1.94	2.23	51.45DBM	.32DB	1.0DB		
		HIGH	-2% to +2%	19,20,21	-7,+7	4.36	5.96	8.92	50.74DBM	.31DB	.9DB		Δ¢ ERROR OFFSET TO 9.0 DEG; RIPPLE IN Δ¢ DATA
MA	5	LOW	-2% to +2%	19,20,21	-6,+6	2.93	2.61	3.71	51.49DBM	.28DB	.8DB	51.1DBM .47DB RMS	INSERTION PHASE ERROR 1°/MHZ
		ROOM	-2% to +2%	19,20,21	-6,+6	3.05	2.75	3.81	51.12DBM	.26DB	.8DB		
		HIGH	-2% to +2%	19,20,21	-5,+7	3.27	3.02		50.49DBM	.25DB	.8DB		
MA	6	LOW	-2% to +2%	19,20,21	-12,+10	6.34	3.79		51.41DBM	.29DB	.8DB	50.83DBM .48DB RMS	PHASE COMMANDS ERATIC
		ROOM	-2% to +2%	19,20,21	-10,+10	5.68	3.29	4.79	51.14DBM	.27DB	.75DB		Δ¢ ERROR ABOUT MEAN 1 TO 2 DEG. TYPICAL
		HIGH	-2% to +2%	19,20,21	-12,+12	6.42	3.24	4.24	50.38DBM	.2DB	.6DB		
RCA	2	LOW	+2%	19,20,21	-20,+12	8.71	----	----	49.6DBM	----	----		AFTER STORAGE AT -55°C
		LOW	0 & -2%	19,20,21	----	----	3.93	6.30	51.18DBM	.14DB	----	50.78DBM .41DB RMS .5DB SPREAD	INSERTION PHASE ERROR 2.5°/MHZ Δ¢ ERROR OFFSET TO 3.38 DEG: Δ¢ ERROR ABOUT MEAN 1 to 2 DEG. TYPICAL
		ROOM	-2% to+2%	19,20,21	-17,+10	8.34	2.78	4.06	51.02DBM	.16DB	.5DB		
		HIGH	-2% to +2%	19,20,21	-17,+10	6.46	2.54	3.83	50.32DBM	.17DB	.6DB		
RCA	4	LOW	-2% to +2%	19,20,21	-7.5,+8	3.96	4.40	8.46	51.72DBM	.29DB	.7DB	51.14DBM .56DB RMS .6 DB SPREAD	Δ¢ ERROR OFFSET TO 8.0 DEG
		ROOM	-2% to +2%	20,21	-7,+7.5	3.43	3.25	6.03	51.40DBM	.22DB	.6DB		Δ¢ ERROR OFFSET TO 5.56 DEG.
		HIGH	-2% to +2%	19,20,21	-6,+5	2.56	3.02	5.13	50.54DBM	.29DB	.7DB		Δ¢ ERROR OFFSET TO 4.65 DEG.
RCA	5	LOW	-2% to +2%	19,20,21	-20,+10	7.92	2.0	3.55	51.35DBM	.36DB	.9DB	50.77DBM .54DB RMS .55DB SPREAD	OVERALL INSERTION PHASE ERROR = 6.36°RMS & .5°/MHz
		ROOM	-2% to +2%	19,20,21	-15,+10	5.90	1.45	1.85	51.2DBM	----	----		
		HIGH	-2% to +2%	19,20,21	-10,+10	4.81	1.45	1.94	50.66DBM	.25DB	.8DB		
RCA	6	LOW	-2% to +2%	19,20,21	-15,+10	5.93	3.19	4.32	51.4DBM	.41DB	1.2DB	51.13DBM .45DB RMS .75DB SPREAD	OVERALL INSERTION PHASE ERROR = 4.85°&1°/MHZ OVERALL Δ¢ ERROR= 2.81° RMS
		ROOM	-2% to +2%	19,20,21	-8,+5	4.34	2.63	3.66	51.32DBM	.28DB	.8DB		
		HIGH	-2% to +2%	19,20,21	-9,+6	4.07	2.56	3.67	50.67DBM	.24DB	.7DB		

NOTE: RCA #1 & 3, MA #2 FAILED - TRANSMIT DATA NOT AVAILABLE
‡SEE TEXT FOR FURTHER DESCRIPTION OF DATA

linear, data similar to that shown in Figures 11A and 11B were derived. Peak and RMS errors for the test conditions are listed in Table III.

5.1.1 RCA MODULES

5.1.1.1 TEMPERATURE EFFECTS

(U) These modules exhibited a change in insertion phase with temperature wherein both the slope with frequency and the offset changed. At center frequency, nominal drive power (+20 DBM) and nominal supply voltages the average insertion phase variation was 0.48°/deg C for the 100°C temperature range but was found to be non-linear ($> 0.48^{\circ}$/deg C from -30°C to $+20^{\circ}$C and $< 0.48^{\circ}$/deg C from $+20^{\circ}$C to $+79^{\circ}$C).

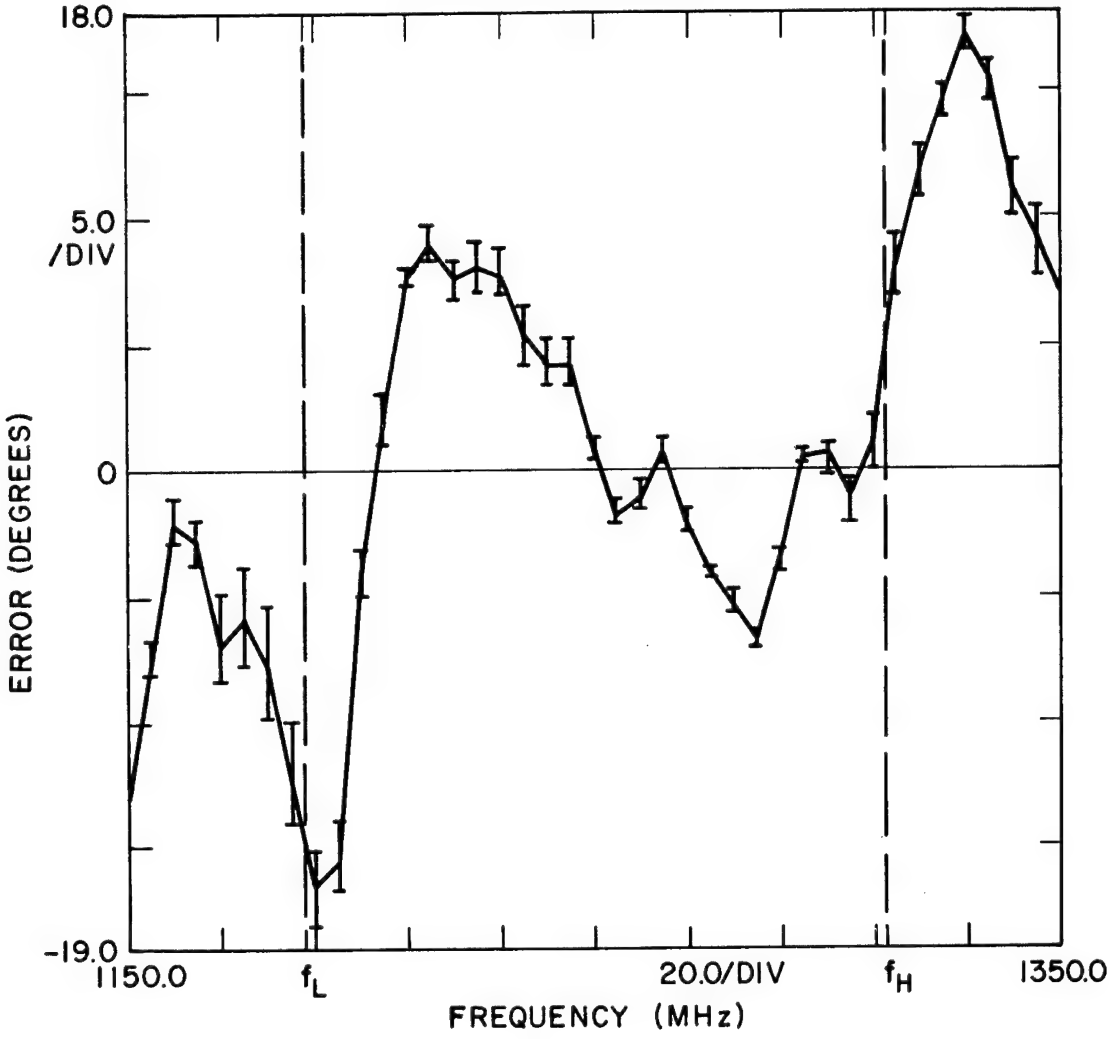
5.1.1.2 DRIVE EFFECTS

(U) At all temperatures the modules exhibited a sensitivity of approximately 1.5°/dB, to input RF drive level. This sensitivity was also found to be a function of frequency, the sensitivity decreasing with increasing frequency with $\frac{\Delta\phi_L}{\Delta\phi_H} \approx 2$, where $\Delta\phi$ = variation.

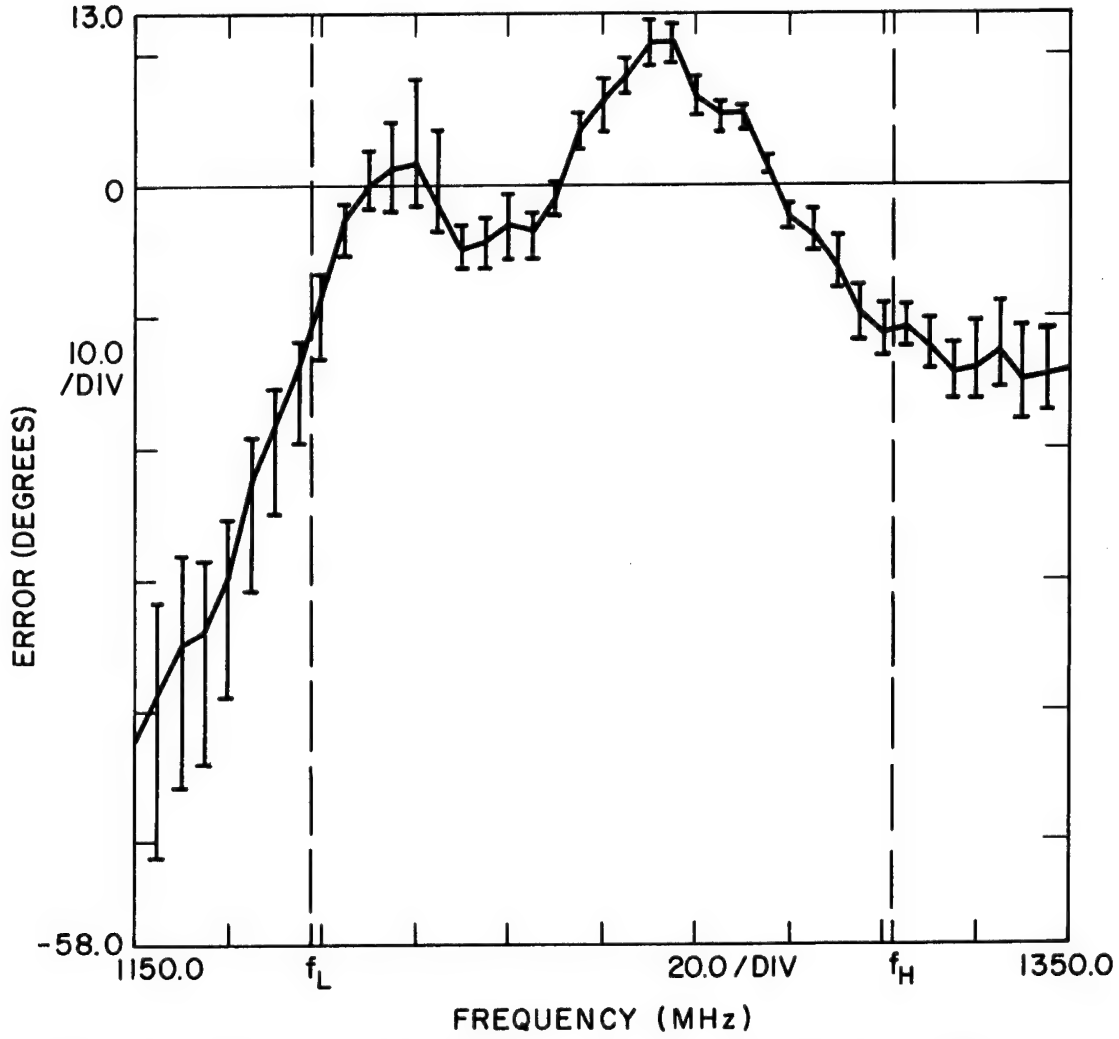
(U) The units evaluated all exhibited an increase in insertion phase length with drive power which was repeatable unit to unit.

5.1.1.3 VOLTAGE EFFECTS

(U) All units exhibited a negligible sensitivity to voltage variations for temperatures between $+20^{\circ}$C and $+70^{\circ}$C. Sensitivity was noted at -30°C but even under this test condition was limited to a maximum value of 1°/% change in voltage.



(S) Fig. 11a - Insertion phase error vs frequency (referenced to linear best fit) (RCA #2, high temperature (+70°C), all voltages and drive levels)



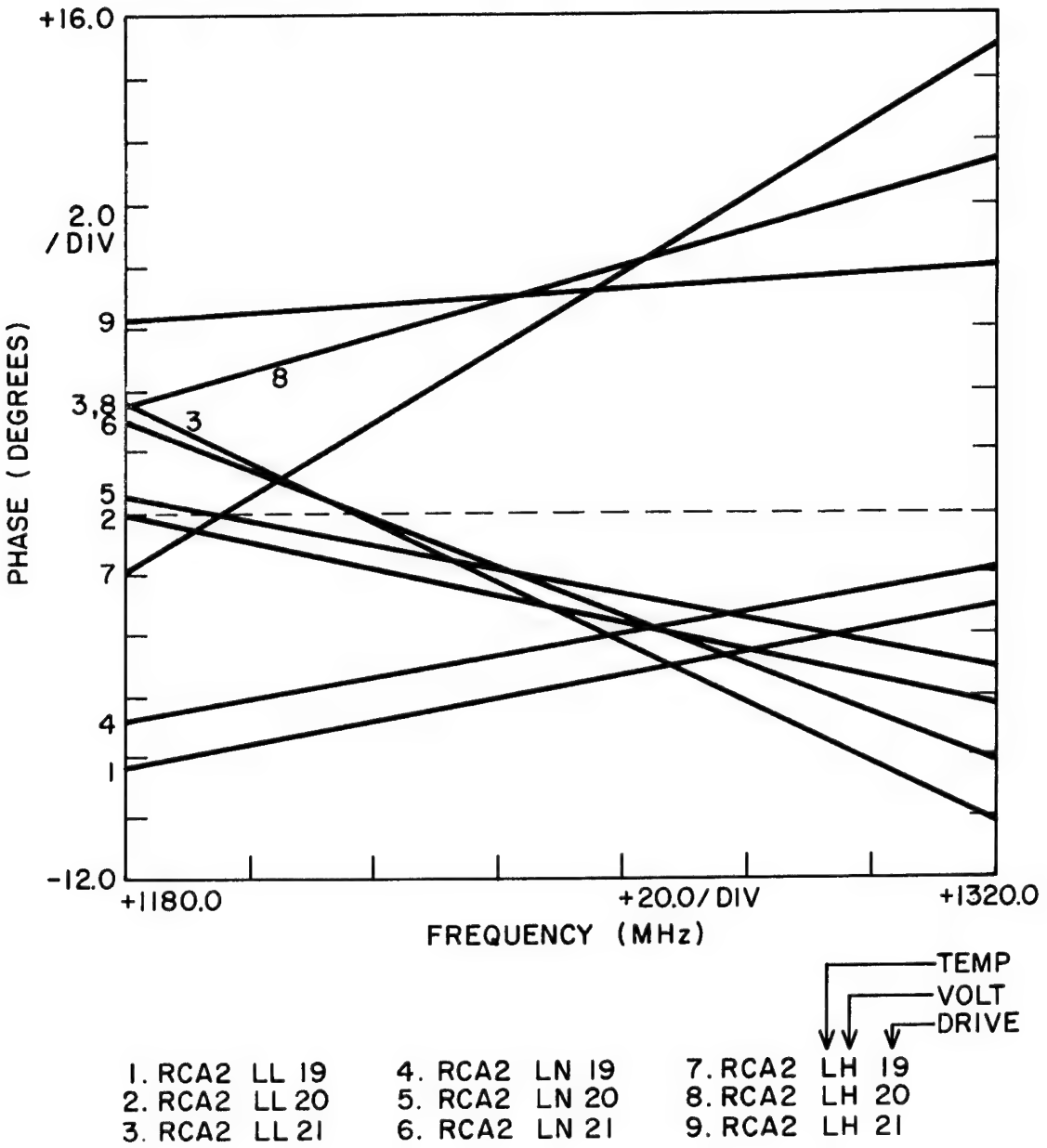
(S) Fig. 11b - Insertion phase error vs frequency (referenced to linear best fit) (MA #6, high temperature (+70°C), all voltages and drive levels)

4.1.1.4 SUMMARY OF INSERTION PHASE DATA - RCA MODULES

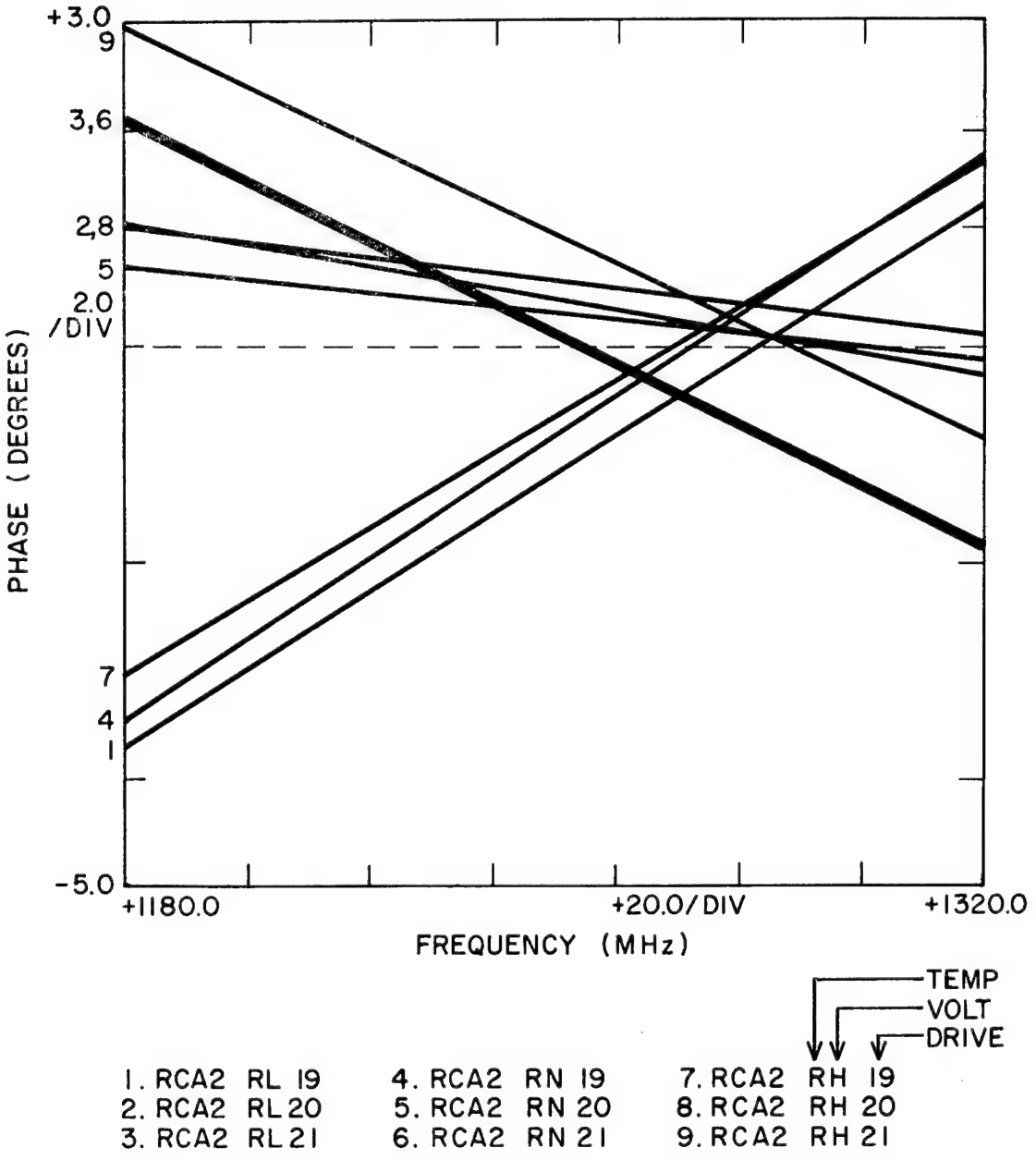
(U) Maximum variation was noted about the test condition of minimum temperature, minimum drive, minimum voltage; and this sensistivity decreased with increase of any and all variables. The inverse variation in insertion phase resulting from drive variations compared to the small voltage variations may result in some slight self-compensation under system operation where power output usually increases with system voltage.

(U) The insertion phase data as derived from measurement for each test condition combination of voltage, drive, and temperature was processed to yield the best-fit linear approximation to the data in the operating band of frequencies. These best-fit approximations were compared in various combinations such that for each combination selected an average line was generated against which variations could be noted; thus the results shown in Figures 12 through 15. From this data trends as a function of individual parameter variations are noted separately from the overlay non-linear errors of the original data.

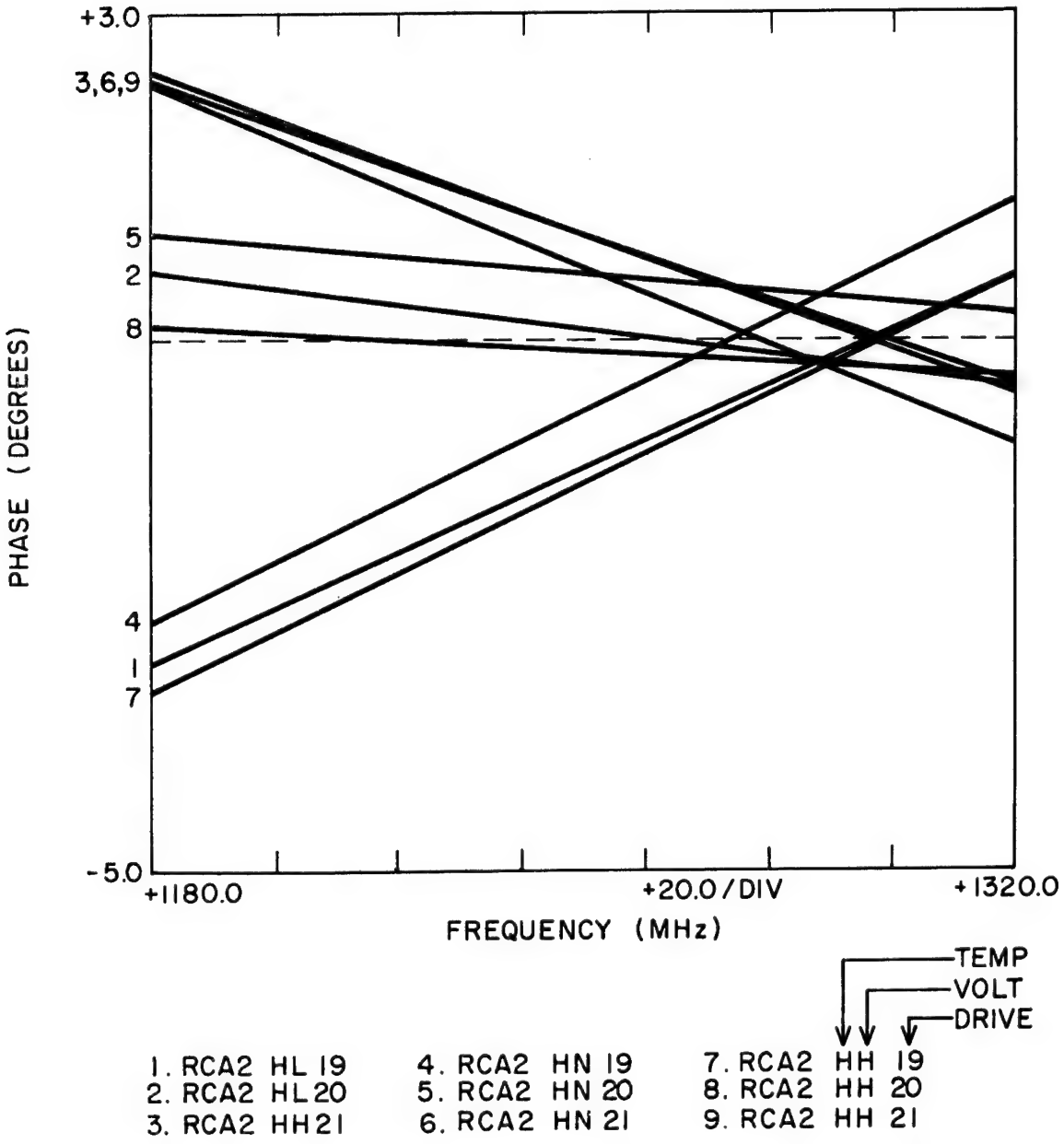
(U) Voltage, drive, and temperature effects are attributed to two causes, physical circuit line lengths and inherent amplifier characteristics. The change of electrical length with temperature (due to actual physical length of the units) should be dependent on the kind(s) of material(s) employed to construct the microwave transmission line (ceramics, metals, etc.) and should be closely repeatable, unit to unit, as is borne out by the data. Amplifier characteristics are less predictable and are heavily design dependent.



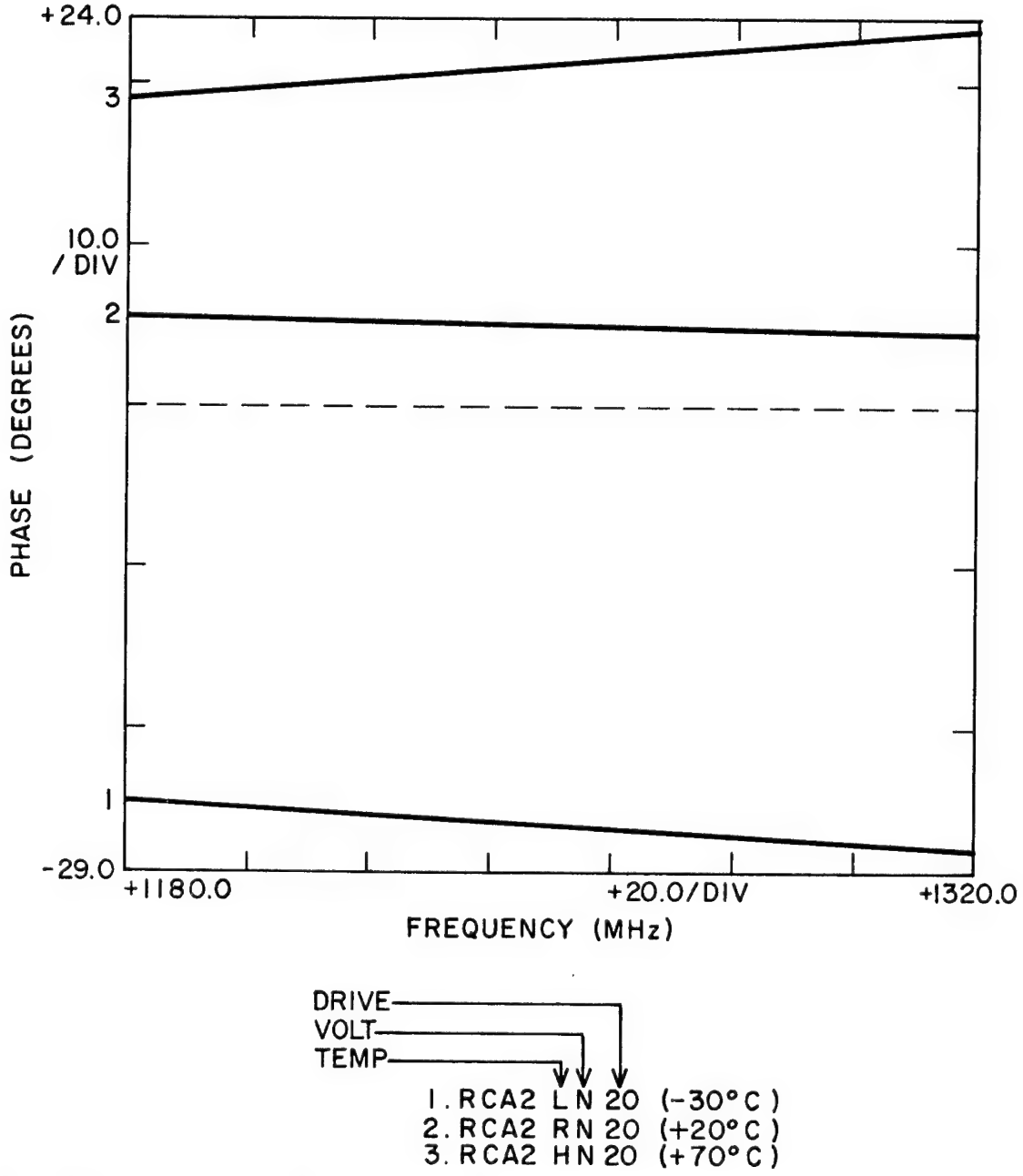
(U) Fig. 12 - Variation in best-fit linear approximation vs frequency for changes in voltage and drive (low temperature (-30°C), RCA #2, transmit mode)



(U) Fig. 13 - Variation in best-fit linear approximation vs frequency for changes in voltage and drive (room temperature (+20°C), RCA #2, transmit mode)



(U) Fig. 14 - Variation in best-fit linear approximation vs frequency for changes in voltage and drive (high temperature (+70°C), RCA #2, transmit mode)



(U) Fig. 15 - Variation in best-fit linear approximation vs frequency for changes in temperature, nominal voltage, and drive (RCA #2, transmit mode)

5.1.2 MA MODULES

5.1.2.1 TEMPERATURE EFFECTS

(U) Assuming nominal voltage and input drive, the insertion phase/frequency behavior of the modules is as anticipated from any air line made from materials that have finite expansion coefficients in the range evaluated. This means that for the equations $\phi = Mf + B$ only the slope M changes with temperature and as would be expected the electrical length increases with increasing temperature. Insertion phase variation with temperature is approximately + 0.5 deg/deg.C at mid-band, nominal voltage and drive.

5.1.2.2 DRIVE LEVEL EFFECTS

(U) Assuming that voltage and temperature are held constant, the module exhibits a sensitivity to drive as a function of frequency. This sensitivity is more noticeable at the low end of the operating band with the change being given by

$$\frac{\Delta\phi_L}{\Delta\phi_H} \approx 2\ \Delta, \qquad \text{where } \Delta\phi = \text{variation in insertion phase.}$$

(U) Data was derived at three temperatures (-30°C, +20°C, +70°C) and it was also found that drive sensitivity decreased with increasing temperature by approximately 2:1 over the temperature range. In all cases the units evaluated became electrically shorter with increase in input drive power.

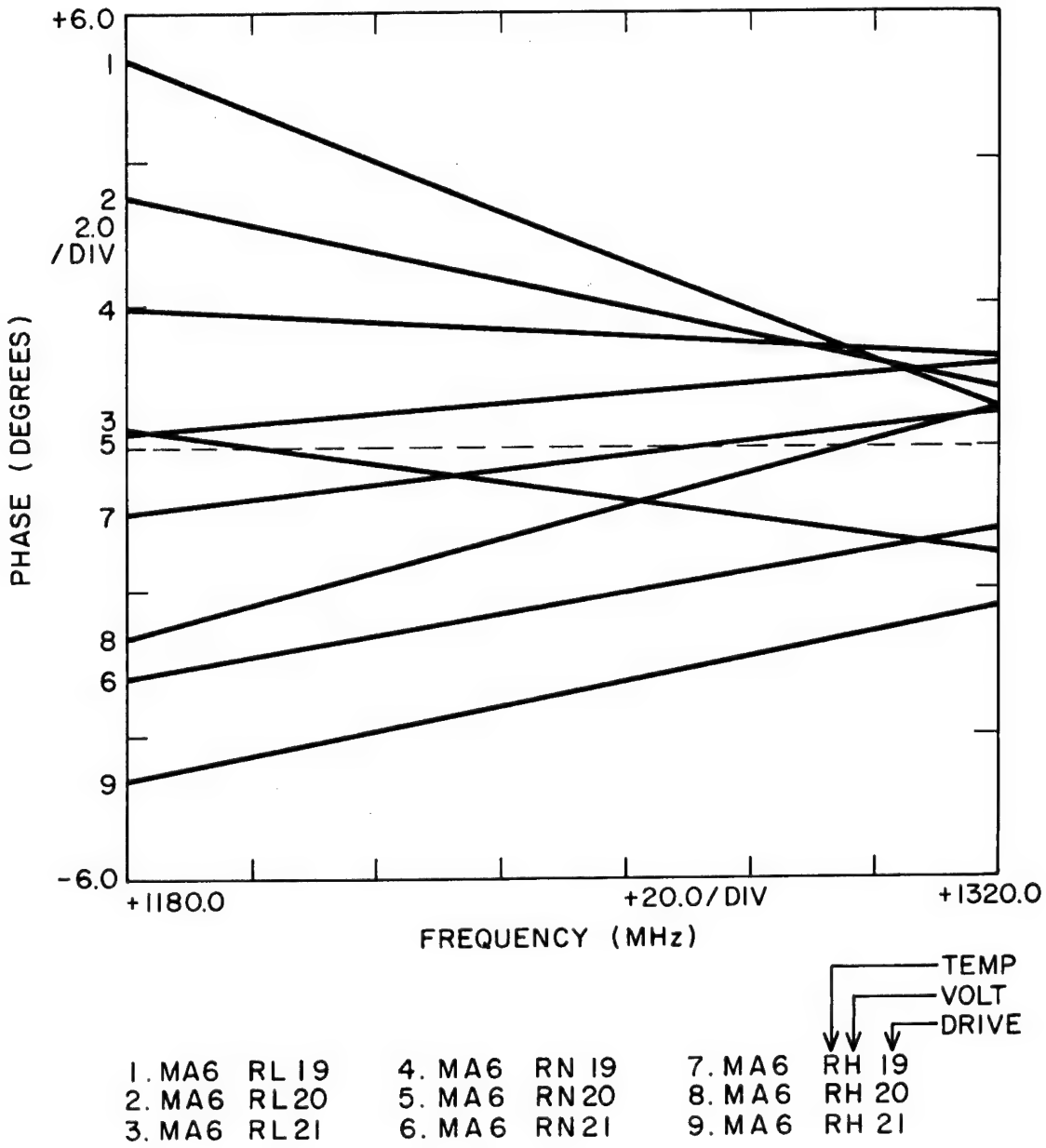
5.1.2.3 VOLTAGE EFFECTS

(U) When holding the parameters of temperature and drive constant, all units evaluated exhibited a decrease in electrical length with increasing voltage. The effects of 4% change in voltage were approximately equivalent to the effects of a 2.0-dB change in input drive power. It was noted that the magnitude of the variation decreased with increasing temperature. The voltage response noted here is reverse from that encountered on the RCA devices and is greater in magnitude than the RCA units.

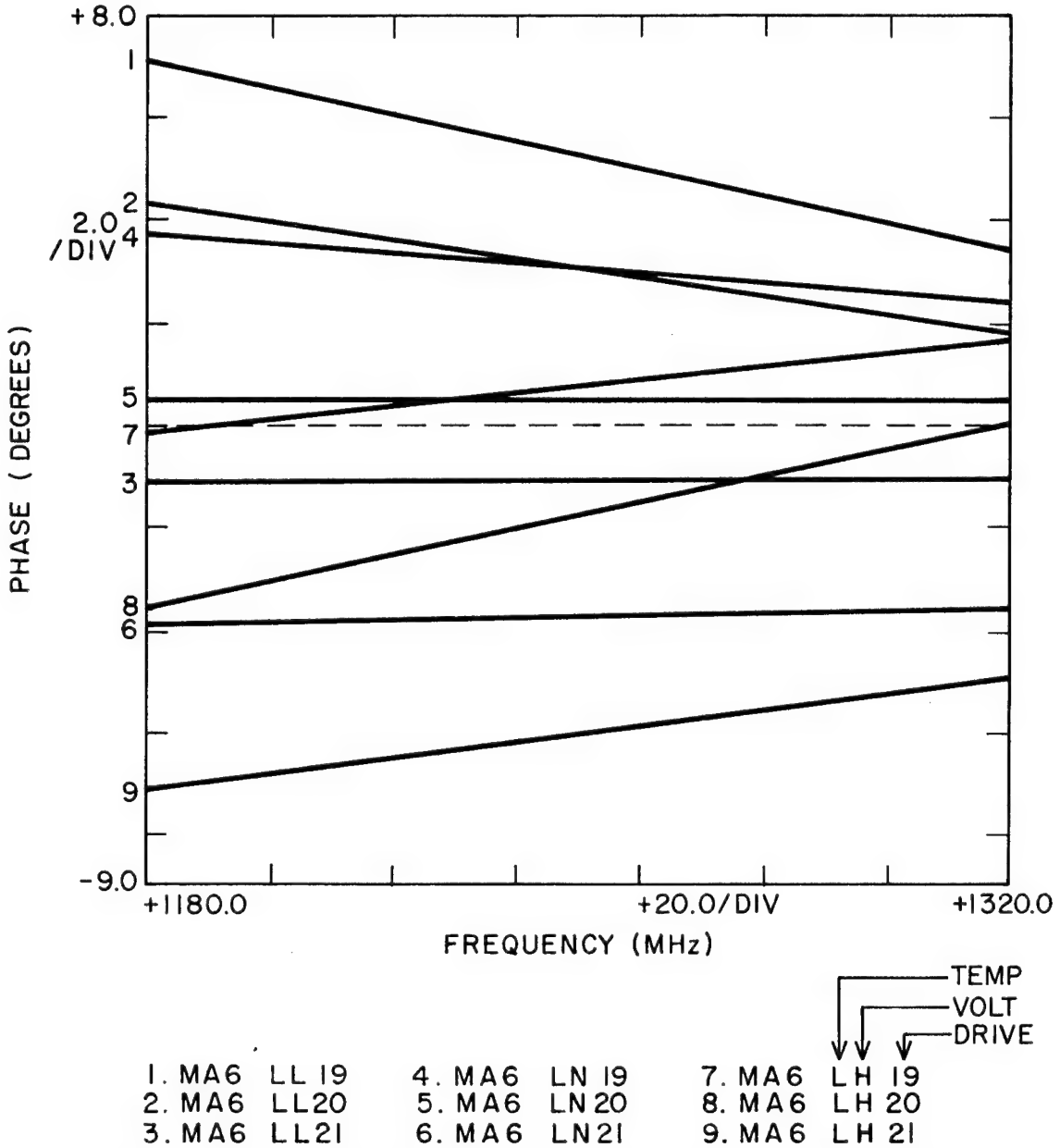
5.1.2.4 SUMMARY OF INSERTION PHASE DATA - MA MODULES

(U) Figures 16 through 19 are representative of best-fit straight-line insertion phase variations noted under various test conditions.

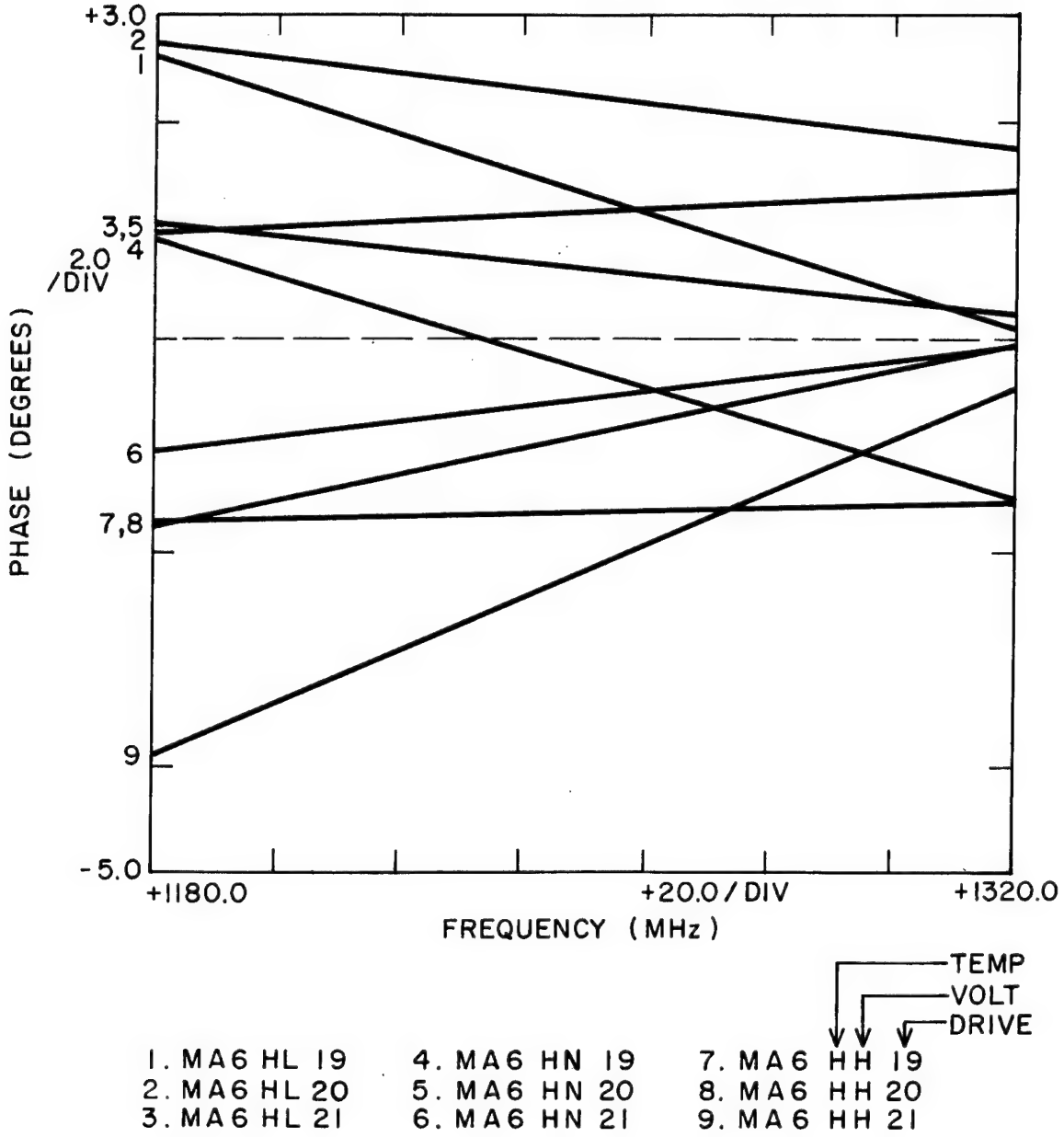
(U) Tests were performed at maximum allowable nominal input drive power (100 mW per specification) $\pm$ 1.0 dB. For these drive conditions, output variations with temperature and voltage were noted that indicate an amplifier dependency to input drive. It is highly probable that the class A amplifier included as part of the module was the major source of the noted variation, and assuming that increases in drive and voltage were permissable (further increases are definitely limited by effects of breakdown, heating, etc.) the variations would be found to decrease as drive and voltage are increased. It is reasoned that these variations are related to compression effects of the class A stage, but this assumption was not verified due to hermetic package construction.



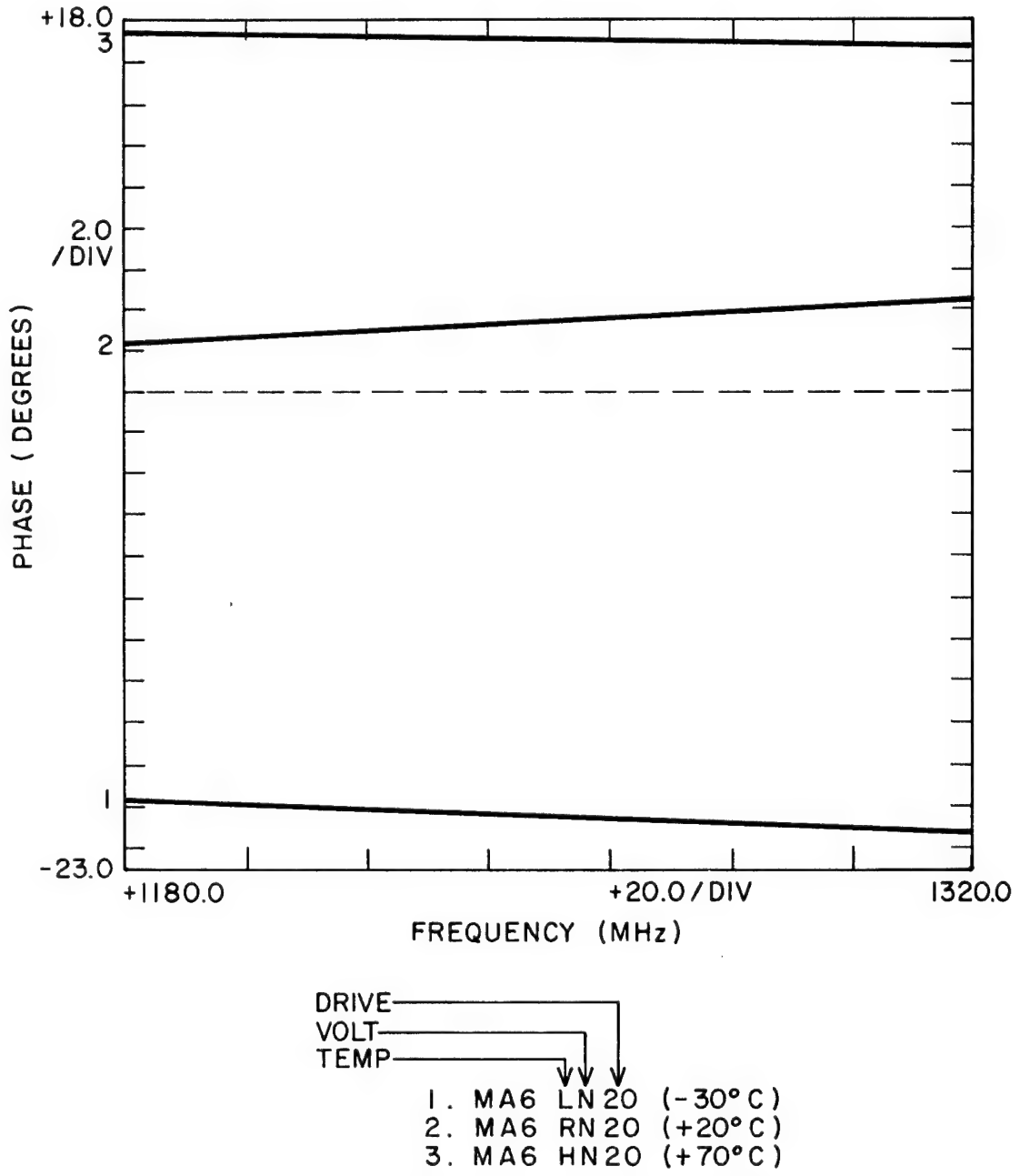
(U) Fig. 16 - Variation in best-fit linear approximation vs frequency for changes in voltage and drive (room temperature (+20°C), MA #6, transmit mode)



(U) Fig. 17 - Variation in best-fit linear approximation vs frequency for changes in voltage and drive (low temperature (-30°C), MA #6, transmit code)



(U) Fig. 18 - Variation in best-fit linear approximation vs frequency for changes in voltage and drive (high temperature (+70°C), MA #6, transmit mode)



(U) Fig. 19 - Variation in best-fit linear approximation vs frequency for changes in temperature, nominal voltage, and drive (MA #6, transmit mode)

Serious consideration should therefore be given to the use of an all-class-C amplifier for applications requiring maximum stability.

5.2 TRANSMIT DIFFERENTIAL PHASE

(U) Each module was exercised through the 16 phase states over frequency, temperature, input RF drive power, and DC supply voltage. The shortest phase state (bit 0) was chosen as the reference state, and all other states were compared to this reference state. The difference in insertion phase between any phase state and the reference state is defined as differential phase. It should be noted that the selection of bit 0 as reference as compared to selection of another state was arbitrary, but once a selection is made, all units used in any actual system must be defined in similar manner.

(U) The phase shifters (the same as those employed in receive mode) in all the modules evaluated are of the line-length variety, which implies that differential phase ($\Delta\phi$) will be frequency dependent. The nominal value of $\Delta\phi$ therefore can be selected at any one frequency in the operating band dependent on chosen line length during development.

(U) The module developers were allowed flexibility in choosing the design frequency for nominal phase, and all evaluation was made against their choice of design frequency. The obtained differential phase data compared to the desired values was studied in the form of peak deviation at each measured frequency, as RMS error at each frequency, and as overall RMS error for all operating band frequencies.

(U) Since array-system operation requires that instantaneously all phase states can exist across the face of the array simultaneously, the error data was always derived as a composite of all 16 allowable differential phase values. Likewise system performance requires that errors be defined from the desired (commanded) value. For purposes of evaluation it was desirous to measure RMS error about the mean error rather than the desired value. As a result of this measurement technique it was found that the mean error contribution to the total system RMS error was as large as the random RMS error about the mean. This mean error appeared as a bias offset whose magnitude was, to a first approximation, bit insensitive.

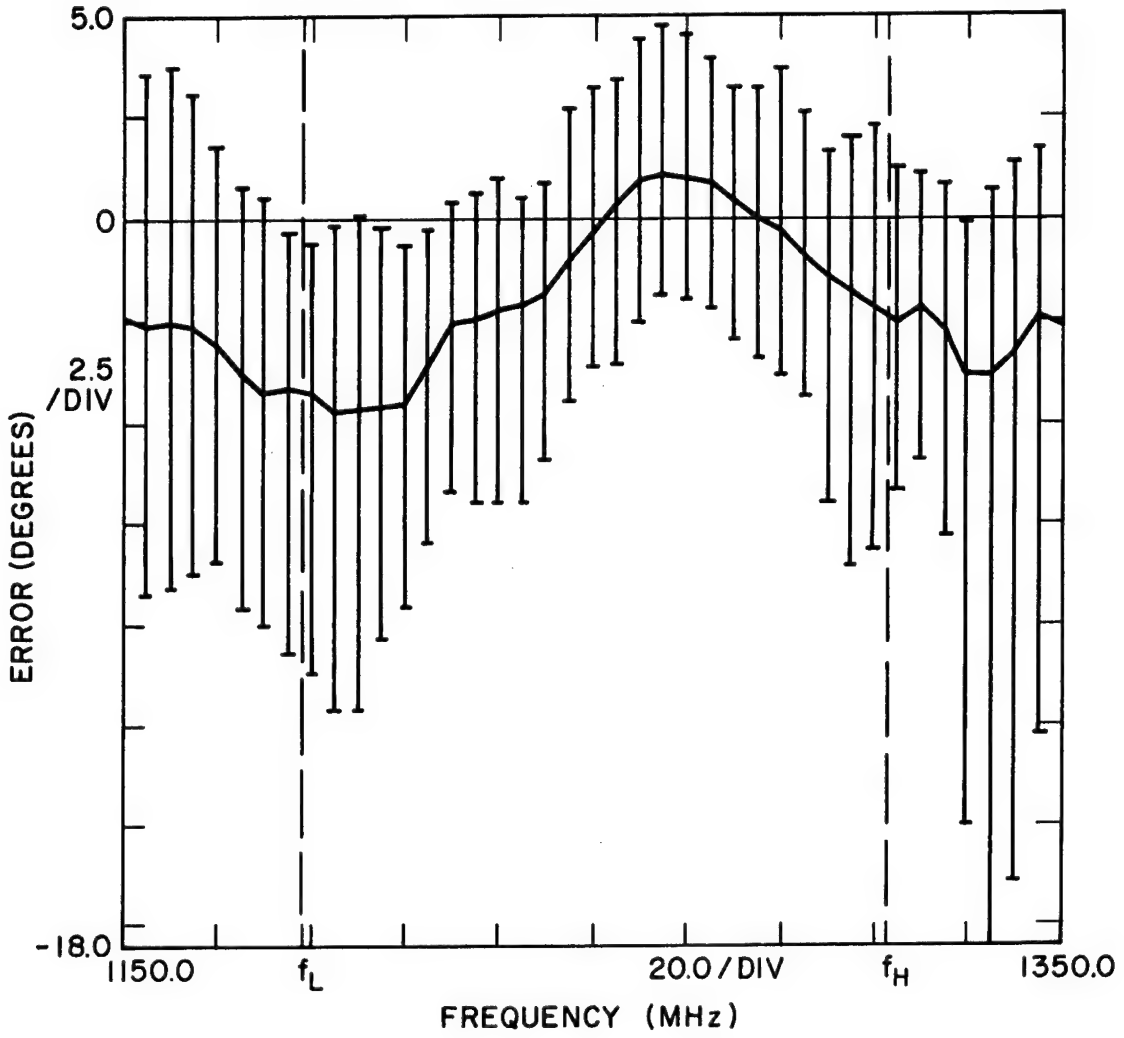
(U) Detail of the error data is given in Table III. This data was obtained from plots similar to those illustrated in Figures 20A and B.

5.2.1 RCA MODULES

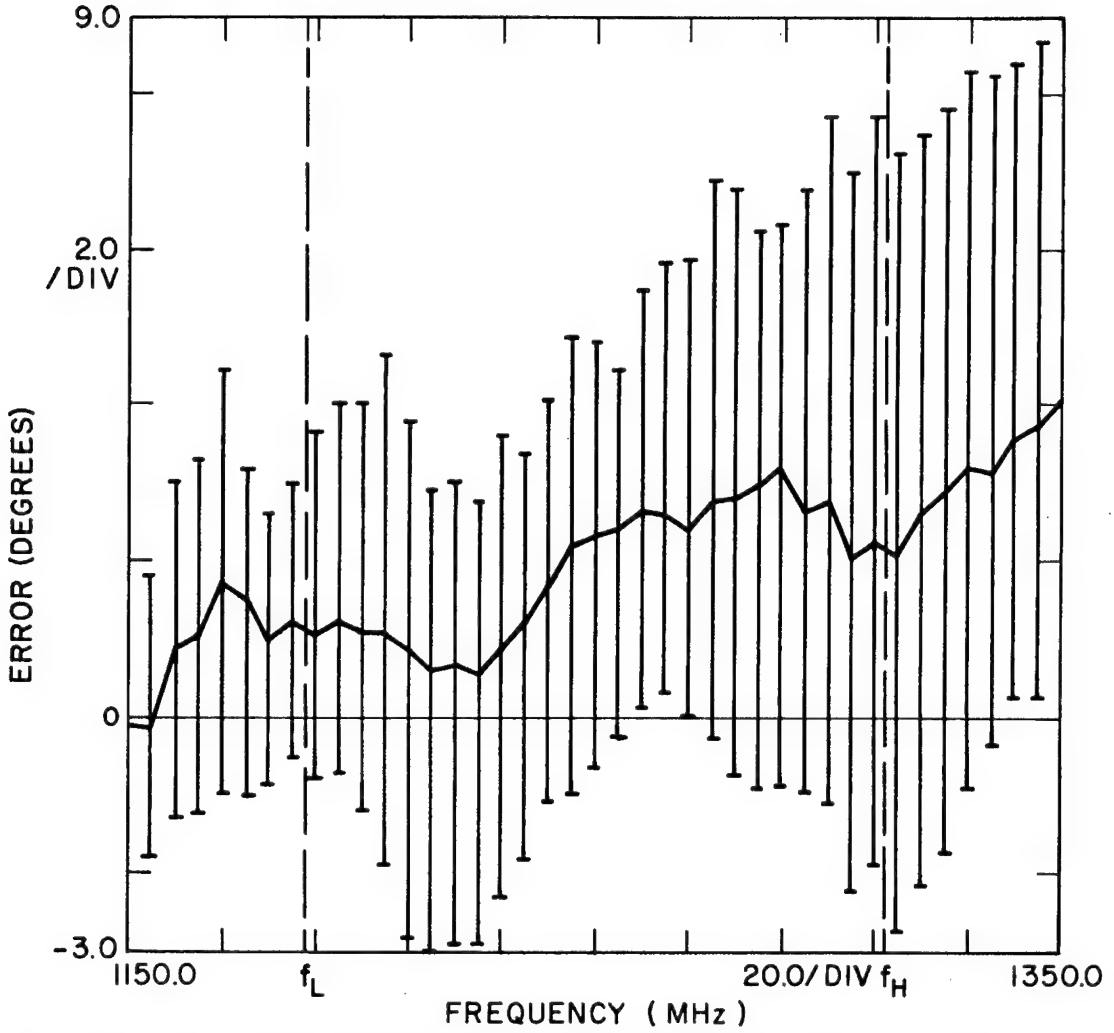
(U) When phase-error offset and RMS error about the mean error are combined to define an overall RMS differential phase error, RCA modules typically exhibited errors of 2 to 5 deg RMS. However when only RMS error about the mean error was considered, these errors were typically 1.5 to 2.5 deg RMS. The offset was not found to be constant nor predictable with frequency; the cause therefore not being associated with improper selection of circuit line length but most likely due to circuit component interaction.

5.2.2 MA MODULES

(U) MA modules performed in a manner similar to RCA modules.



(S) Fig. 20a - Differential phase error vs frequency for all phase states, drive levels, and voltages (high temperature (70°C), RCA #4, transmit mode)



(S) Fig. 20b - Differential phase error vs frequency for all phase states, drive levels, and voltages (room temperature (+20°C), MA #3, transmit mode)

Except for erratic phase control at low (-30°C) temperature for some of the modules evaluated, individual error data points were below the limit level of ± 10 degrees. Erratic behavior of phase control is most likely due to logic malfunction and thus would not be associated with RF circuit component failure.

5.2.3 OTHER SOURCES OF ERROR

(U) It was found that variations in differential phase error with temperature, supply voltage, and drive power existed but were not always predictable, unit to unit. This randomness was most noticeable with the MA modules, whereas in general some small improvement in RMS error with increase in temperature was noted for the RCA modules. Any change in performance however was small compared to the base-line random and offset error.

5.3 OUTPUT TRANSMIT RF POWER

(U) Because of the need for thermal control during transmit operation, all testing was performed with the unit under test attached to a suitable cold plate. Air cooling was used at all temperatures to control cold-plate temperature. In accordance with the suggested test methods of the various module developers, one specific module interface surface was designed a thermal transfer surface. Internally the transmitter transistors, in particular the high power class C output stages, are thermally coupled to this surface. Externally this surface is attached to a system cold plate during operation.

(U) The requirement therefore imposed on the modules under evaluation was not control of ambient temperature but rather the temperature of this transfer surface. Depending on the cooling surface efficiency and the thermal transfer characteristics of the attached cold plate, the required ambient, and therefore the temperature to which the remainder of each module (other than transfer surface) was subjected, varied from manufacturer to manufacturer.

(U) It was found that using a flat (no fins) 3/8 in. thick x 1 ft^2* aluminum plate attached to the MA modules resulted in a transfer surface to ambient gradient of 8 to 10°C. MA used one entire surface of the module for transfer, whereas RCA restricted the heat transfer area to bosses located at strategic points on the surface. In each case the thermal transfer area of the cold plate (supplied by RCA) was less than the 1 sq. ft mentioned for MA, but the cold plate was finned to increase effective transfer area. The gradient between the thermal surface of the module and ambient for the RCA units varied from 20 to 30°C.

(U) This variation, manufacturer to manufacturer, in test conditions is stressed because this obviously places an additional perturbation of unknown magnitude on all test results. It was decided however that each manufacturer should be allowed full flexibility in design of cooling structures, and this choice included cold-plate design. Data on each design is on file including positioning relative to air circulation, so that detailed thermal studies to specific system requirements can be made as required.

*95 mm thick x 0.093 m^2.

(U) The only test restriction placed on each manufacturer was that only the designated thermal transfer surface would be maintained at specified temperature, the remainder of the module being subjected to whatever ambient resulted after thermal stabilization.

(U) It has been found that a design limitation relative to cold-temperature operation has been inadvertantly incorporated into all modules. To attain minimum size and weight the RF circulator (incorporated into all modules) employs ceramic magnets that when cooled beyond some critical temperature (for the devices incorporated into these modules, this temperature is -35°C to -40°C) exhibit a irreversible decrease in magnetic properties. This doesn't imply that the device is destroyed, the magnets can be recharged to their original strength when the unit is again returned to acceptable operating temperatures. This however does specifically limit the minimum temperature experienced by the circulator from any and all causes to -30°C without degradation.

(U) This then implies that operation in an ambient environment below -30°C is subject to high risk. Under the test conditions, cold-plate temperatures were maintained at -30°C with the unit operating. This required that the chamber ambient air temperature be decreased to a range of -40°C to -55°C. If for any reason the module was placed in standby or off mode while under this environment, the cold plate and therefore the entire module temperature attempts to reach equilibrium with the environment; and such temperatures create unacceptable circulator conditions.

(U) Every indication therefore points to a need for circulator redesign if system conditions indicate a possibility of operation or storage below -30°C. This redesign can be extended to cryogenic temperatures by selection of proper magnet materials but in all cases will result in increase in size and weight (≈ 30% increase in size for operation to cryogenic temperature) of the circulator.

(U) In addition to circulator degradation below -30°C, and as a result of phase command errors noted in some MA units at -30°C, it is postulated that careful consideration must be given to all device components at temperatures below -30°C. This consideration is not oriented towards storage nor is there necessarily an operating specification limit implied below -30°C. It must be determined (the present design limits the pursuit of this task) if the device as designed will reach some temperature where turnoff occurs, and considering heat rise effects, there may be a temperature below which the device can not be turned on within the limits of RF drive. This does not imply physical damage (such as cracked substrates, etc.) but such possibilities as detuning of RF circuits, or inability of the logic to apply bias voltages. This condition was encountered on one RCA unit. Admittedly, the test was far below normal operational frequencies where circuit elements were not optimized. As the temperature was decreased, with the unit fully operational (RF drive, all voltages on, RF power output) a temperature was attained where the RF pulse was slow to turn on (10's of micro-seconds turn on). This slow turn-on caused a decrease in average dissipation which further reduced internal temperatures, resulting in a run-away condition. The reverse behavior occurred as ambient

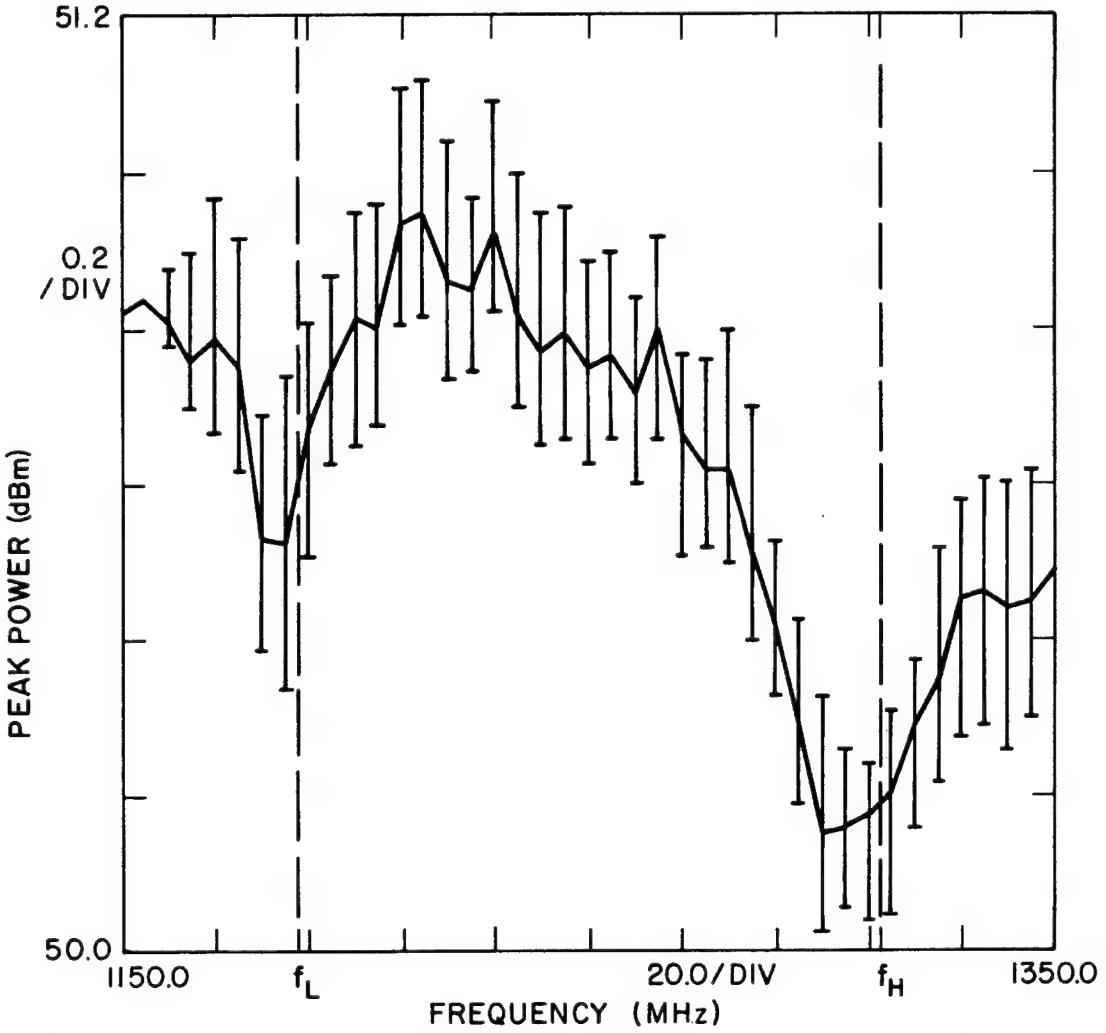
temperature was increased.

(U) Such conditions could be encountered within the normal design operating band at colder temperatures, and if such temperatures are anticipated under system start up or operate modes, then all components must be subjected to further consideration.

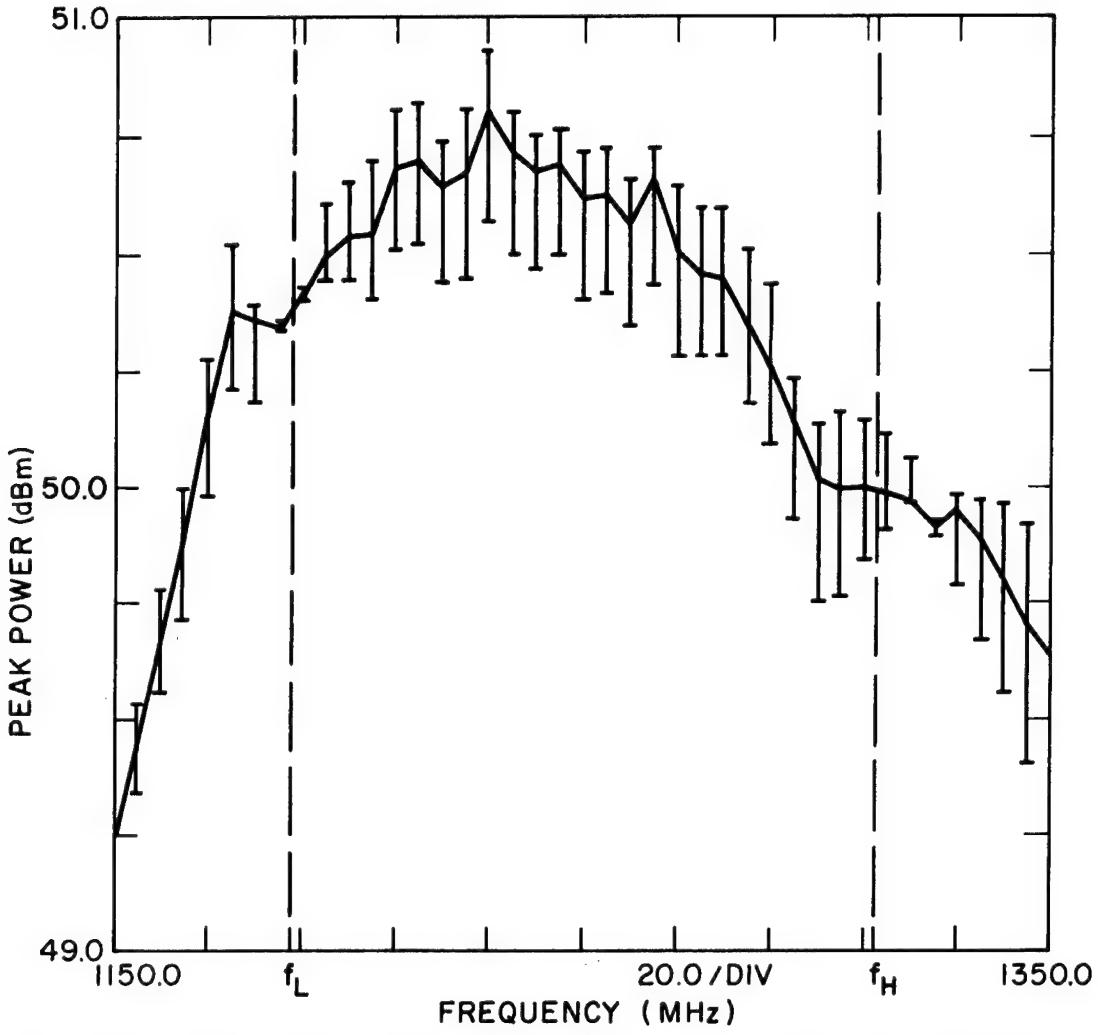
5.3.1 DEFINITIONS

(U) Guideline module specification requirements were imposed upon the module developers. Most of these specifications have a clear definition not only in terms of method of test evaluation but also with regards to system performance. There were however several specifications with regards to output power that are heavily dependent on system functional use. It was therefore decided to give the test data without any reference to specification quality other than to define the measurement terms.

(U) Figures 21A and 21B are typical plots of power output (in DBM) vs frequency. Test variables could include temperature, voltage, and drive, but always the test condition included evaluation at 16 phase conditions. The resultant data therefore yields maximum and minimum peak power at each frequency and average peak power for all 16 phase states. Figure 22 is a sample tabulation of average peak power at each frequency and the RMS spread about this average peak value. The data therefore is complete in itself and only awaits the system application for interpretation of bandwidth and rate of change in power with frequency.



(S) Fig. 21a - Peak power output (dBm) vs frequency for all phase states, all voltages, and all drive levels (high temperature (+70°C), RCA #5, transmit mode)



(S) Fig. 21b - Peak power output (dBm) vs frequency for all phase states, all voltages, and all drive levels (high temperature (+70°C), MA #5, transmit mode)

FREQ	MA-6-R PEAK AVG.	MA-6-R OUTPUT RMS	RCA-6-H PEAK AVG.	RCA-6-H OUTPUT RMS
1150	49.53	.05	50.92	.04
1155	49.83	.04	50.94	.08
1160	50.10	.07	50.95	.13
1165	50.47	.11	50.95	.12
1170	50.67	.00	50.96	.09
1175	50.91	.09	50.93	.08
1180	50.89	.08	50.73	.09
1185	51.02	.11	50.71	.08
1190	51.18	.14	50.78	.08
1195	51.23	.14	50.01	.09
1200	51.23	.14	50.83	.08
1205	51.18	.13	50.79	.07
1210	51.26	.13	50.91	.08
1215	51.24	.13	50.92	.07
1220	51.18	.12	50.84	.08
1225	51.22	.13	50.06	.09
1230	51.40	.12	50.96	.08
1235	51.36	.12	50.05	.08
1240	51.37	.14	50.81	.08
1245	51.41	.14	50.83	.09
1250	51.35	.16	50.77	.09
1255	51.34	.14	50.79	.08
1260	51.25	.16	50.74	.08
1265	51.32	.16	50.80	.08
1270	51.17	.16	50.57	.08
1275	51.12	.16	50.44	.08
1280	51.10	.16	50.47	.05
1285	50.99	.15	50.46	.08
1290	50.91	.14	50.43	.07
1295	50.79	.12	50.33	.09
1300	50.64	.15	50.23	.09
1305	50.63	.12	50.26	.08
1310	50.64	.16	50.34	.09
1315	50.69	.15	50.41	.08
1320	50.67	.16	50.46	.07
1325	50.59	.15	50.42	.08
1330	50.58	.16	50.48	.09
1335	50.55	.14	50.47	.08
1340	50.45	.15	50.45	.08
1345	50.41	.15	50.46	.11
1350	50.40	.14	50.49	.13
AVG. OVER ALL OPERATING BAND FREQUENCIES	51.14	.27	50.67	.24

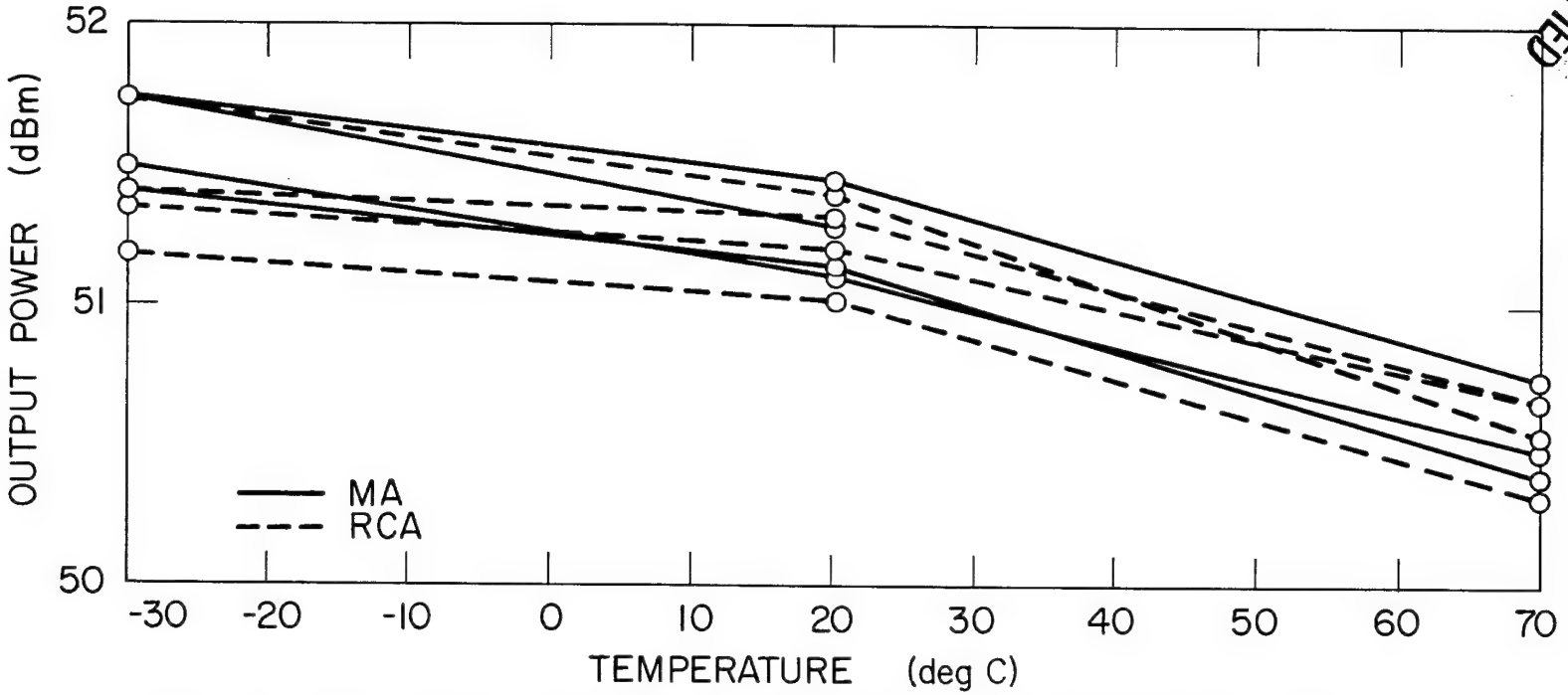
(U) Fig. 22 - Average value of peak power (dBm) and RMS variation about average, value (dB) vs frequency for all voltages and all drives (MA #6, room temperature, RCA #6, high temperature)

(U) Table III also gives average peak power values over broader test conditions. Wherever available, three kinds of data are listed:

1. Average peak power in DBM averaged over operating band frequency and 16 phase states in addition to any variables listed.
2. The RMS distribution in power about this average peak value in DB.
3. The spread (maximum to minimum) of the average peak value encountered in the operating band.

Figure 23 is a plot of average value of the peak power (averaged over frequency, drive, voltage, and phase) as measured at 3 temperatures for several modules. It is interesting to note that power output is not linear over the operating temperature range, and that similar characteristics have been noted from independent module suppliers. Investigation of the detail data also showed that the temperature power profile was independent of input drive level, and closely followed the data of Figure 23 for drive levels of 19, 20, and 21 DBM.

(U) It is especially interesting to note that the final value of peak power, derived for each module supplier, averaged over all test parameters and in addition averaged over all units available for test, was the same for each source; the value being 124 watts peak. In addition the distribution in power about this averaged value for the various test conditions was .47 dB RMS for Microwave Associates and .49 dB for RCA, the difference between sources being neglibible.



(U) Fig. 23 - Average peak power vs temperature averaged over phase state, input drive, and voltage for various transceivers

(U) This implies that a module controlling factor other than circuit design is the limiting state-of-the-art consideration, since each developer used different make transistors. This limiting factor is reasoned to be the physics of the transistor driver itself.

5.4 TRANSMIT PULSE DROOP

(U) The peak pulse current required by a typical module for proper transmit operation is in excess of 15 amperes. It becomes impractical to expect the DC power supply to deliver this peak current directly. Likewise, I^2R and inductive losses would cause large voltage excursions at the module if long power-distribution cables are used alone.

(U) A solution to the problem of supplying sufficient peak current while maintaining a closely controlled voltage has taken the form of:

a. The manufacturer placing storage capacitors within the module as close to the output transistors as possible.

b. Adding large storage capacitance external but close to the module.

(U) All modules were evaluated using 32,000-microfarad capacitors external but as close to the module (usually within 2 inches*) as possible. The resistance of the power cable from the capacitor back to the supply was sufficient to limit the average supply current to under 3 amperes at all times. Under these conditions, power supply regulation and current limiting problems were essentially eliminated.

(U) Some voltage drop was experienced along with voltage droop during the pulse. The resistive/inductive characteristic of the capacitor

*Approx. 5 cm.

resulted in a voltage drop or bias of approximately .5 volt. The droop at the external capacitor was found to be small, but this did not in any way guarantee that the voltage at each transistor internal to the module was fixed.

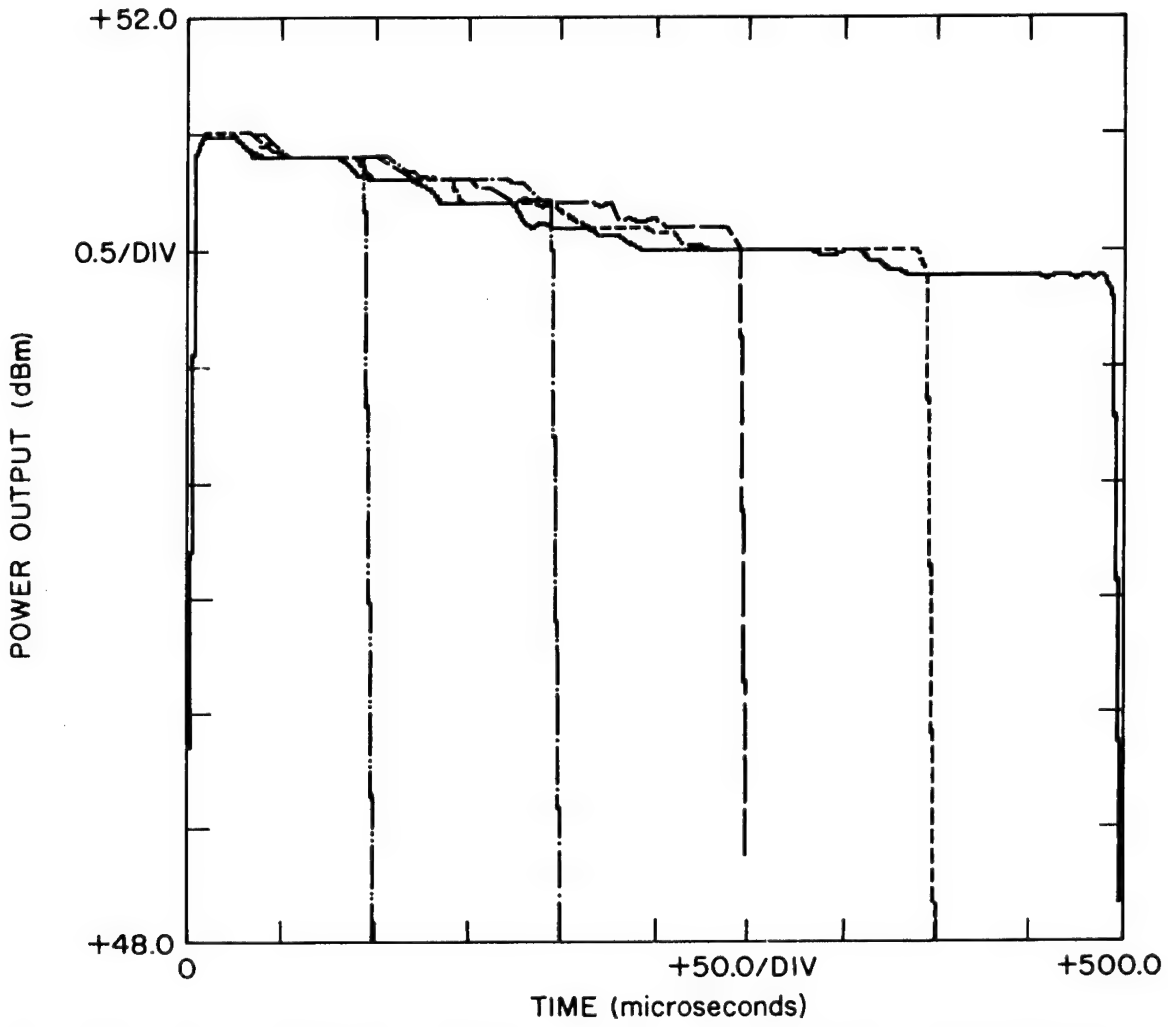
(U) Any variation in voltage at the output transistors from all causes is translated to the RF output as a variation in RF power with time during the pulse.

(U) In addition to RF power variation with time due to power-supply characteristics, the RF output is dependent upon the instantaneous temperature of the various transistors during the pulse, where the gain of the amplifier varies with temperature. This temperature variation is due to dissipations within the devices and thermal impedance of the devices. Not only is there an intrapulse perturbation in temperature, but the magnitude of this perturbation is dependent on base temperature, since the conductivity of the transistor material is non-linear. Figures 24A and 24B are composites of several plots of peak power as a function of time where pulse length was varied.

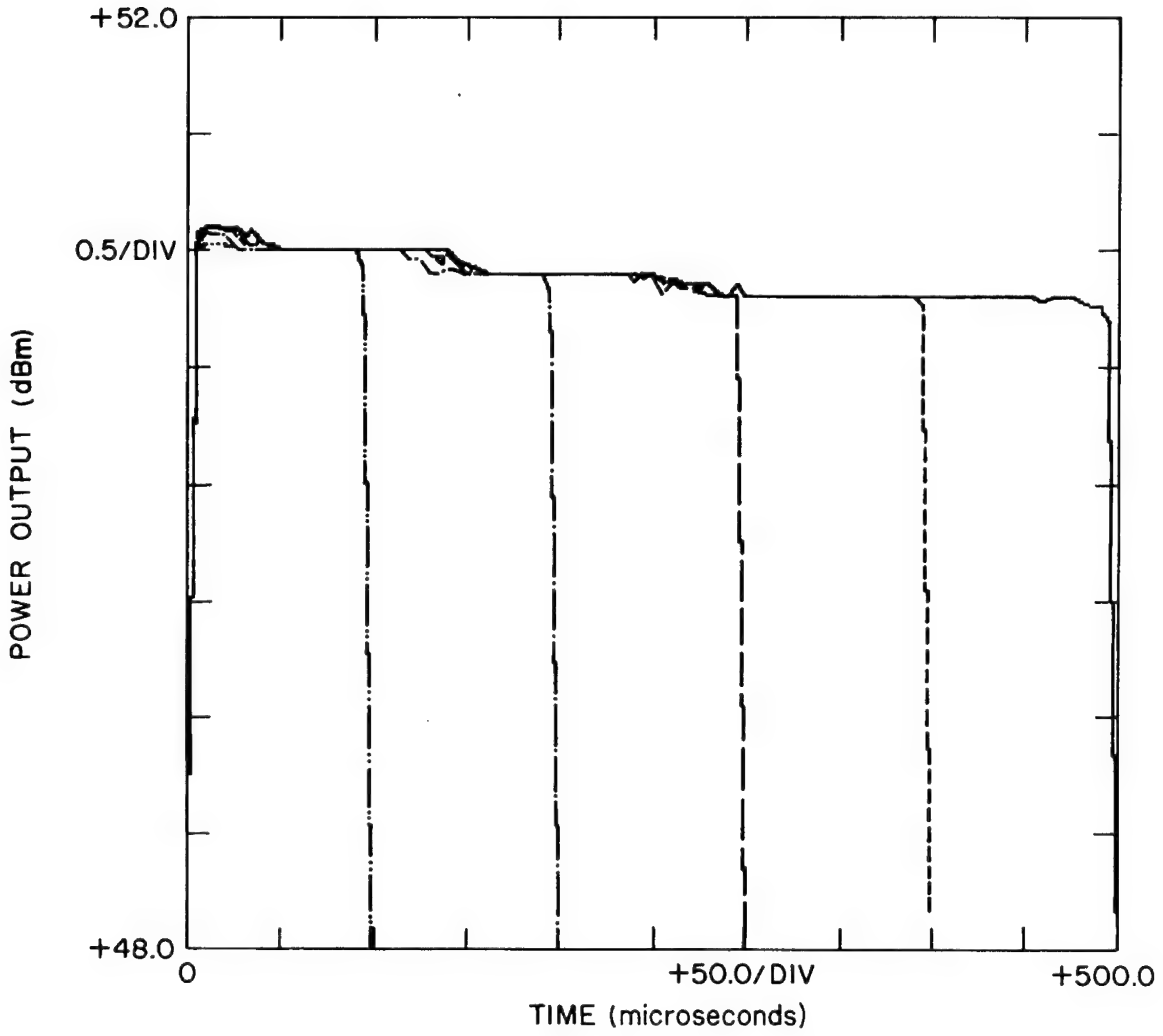
(U) The magnitude of this droop during the RF pulse can be anticipated as typical for RF transistor amplifiers. Some precautions can be incorporated into the device design to minimize this effect, but complete stabilization appears impractical at this point in time.

(U) Attempts were made to relate overall transceiver behavior to individual transistor behavior. Correlation was unacceptable and was influenced by such parameters as

a. Several different transistor designs in single package;



(U) Fig. 24a - RF output vs time (RCA #5, f = 1250 MHz, 20-dBm drive, room temperature, nominal voltage, PRF set to 200)



(U) Fig. 24b - Output power vs time (MA #20, f = 1250 MHz, 20-dBm drive, room temperature, nominal voltage, PRF set to 200)

b. Effects of temperature on tuning of circuits;

c. Transistor impedance changes with temperature.

5.5 TRANSMIT ISOLATION

(U) As described in Section 4, isolation of the transmit and receive sections of the transceiver is necessary to assure stable operation.

(U) The transceiver was placed in transmit mode for evaluation of isolation, but RF was injected into the antenna port (normal transmit output).

(U) Under these test conditions, typical isolation was found to vary with frequency, over the operating band from a minimum of 47 dB to a maximum of 67 dB.

(U) In all instances the isolation was much in excess of specification requirements and should prove to be adequate for all presently envisioned applications of these devices.

6.0 RELIABILITY

(U) The purpose of this program was not explicitly directed towards reliability, but implicitly, each supplier was expected to develop a device that would be capable of long-term operation in a rugged environment without maintenance.

(U) So, as a matter of policy, materials and processes were chosen that had the basic characteristics necessary for high reliability.

(U) There are however electrical components existing within the device that have at present only limited reliability testing. In addition, because of the complexity of the microwave circuitry, it is often not possible to predict with accuracy the stress levels that will be encountered prior to actual hardware test.

(U) It is therefore reasonable in a device as complex as the transceiver module to expect failure modes to appear during initial evaluation.

(U) The microwave transceivers developed by both RCA and MA experienced failures during the evaluation phase of the program. In almost every case however the failure mechanism could be categorized and a specific area of further investigation could be defined; the failures were not random.

6.1 FAILURES

(U) The following failures were noted:

A. RCA - of 6 units subjected to evaluation, 2 units failed during test:

Serial #1: Failure - logic circuit;

Action - replace;

Cause - unknown.

Serial #3: Failure - logic circuit, and TA8777 power amplifier transistor;

Action - replace both components;

Cause - unknown.

- Removal of the logic circuit results in its destruction. To properly isolate the fault mechanism may require that the circuit be stressed separately from the device in a manner that probing can be performed without destruction.
- Only one transistor failure occurred, and until further statistics are available no prediction of the failure mechanism can be made.

B. MA - of 5 units subjected to evaluation, 4 units failed during test:

- 2 units failed under transmit test conditions. Analysis indicated the overstressing of an intermediate class C driver amplified stage.

  Analysis of the test conditions yield, as a possible cause, excess input drive power resulting in dissipation beyond the limits of the device. Such input power levels were chosen to simplify evaluation over a large

band of frequencies. Future testing will be restricted to reduced input power over only the design operating band.

- Two units failed during receive evaluation. One unit showed intermittent behavior.

  Analysis of the circuit indicated failure of circuit bonds which, when repaired, resulted in return to operation. These were physical failures probably associated with temperature cycling. Better process control and/or new bonding techniques are indicated.

Such failures are to be expected, although not desirable, and to this extent the program can be considered successful in pointing out deficiencies of design or processing that require further investigation.

7.0 CONCLUSIONS

(U) The most general conclusion centers on the fact that practical L-band solid-state transceiver modules can be designed and manufactured to meet actual system needs. This statement therefore also implies that the various major transceiver module building blocks (receiver, transmitter, phase shifter, T/R switch) are also manufacturable.

(U) This general statement should not be interpreted to imply that all components have been optimized. The transceiver modules are believed satisfactory; not perfect.

(U) Several times throughout this report, it was mentioned that as a result of thorough evaluation of the overall transceiver module, the test data indicated a strong need for further investigation at the device or circuit level within the modules. The present program was not organized to permit such investigation, but, nevertheless, the need for such investigations are indicated. It can only be concluded that until such time as each parameter exhibiting some unexpected but important characteristic is better understood and, more importantly, from the users standpoint, is controllable, that the full scope of this program is yet incomplete.

(U) Likewise the nature of the program was such that the module developers were permitted some flexibility in their specific choice of design approach. This flexibility coupled with the general desirability of a multiple-use design led to the inclusion of circuitry and components in the delivered hardware not necessarily indicated by the governing specification. This was especially notable in the

logic areas. This coupled with ill-established engineering model quality control procedures undoubtedly resulted in a reduction in reliability and higher failure rate.

(U) This should not be construed to imply that interchangeability and universality of components and subassemblies are not desirable. It does imply that the techniques employed to reach the state of universality should be such that the specific application design and reliability should remain a prime focus. The use of universal building blocks and standard logic chips is a desirable goal, but from the very limited evidence of this program this universality where applied has created an unproportionately large deficit in reliability.

(U) The obvious question of this program, can modules from several sources be mixed, remains to be answered. With the limited data available, the answer can only be "maybe". Certainly with the obvious difference in electrical and physical characteristic presently existing between sources, these modules are not interchangeable; but likewise there are startling similarities in performance, the most noteworthy being overall transmitter peak power and variation about this nominal value.

(U) This similarity does not imply interchangeability however but only a possibility in the future. If specifications are sufficiently detailed and a single design is chosen for all production units it is highly probable that multiple manufacturers can be chosen.

(U) It should also be mentioned that to assure a high confidence level during development and likewise to optimize test during production,

thorough retest and evaluation should accompany any redesign. Some judgement obviously must be applied as to what constitutes redesign, but when the complexity and overall interaction of the various parts of the device are considered, even small areas of redesign can create large and unpredictable changes in performance.

7.1 RECOMMENDATIONS

(U) In summary, this program was quite successful in its goals for Phase I and II; despite the enormous quantities of data gathered, from a statistical viewpoint, "the surface was barely scratched". In addition large areas of very important peripheral information were completely ignored due to time limitation. The following recommendations are therefore made:

- Procure and evaluate more modules to improve accuracy of present data and statistics of performance.
- These modules should incorporate key changes as derived from further development in:
    - logic and RF transistor reliability,
    - operation at cold temperatures,
    - transmit insertion phase linearity,
    - VSWR stability.

- DC, Low voltage/high current distribution methods merit further investigation and should include:

  size,

  weight,

  number of voltages and accuracies,

  failure modes.

APPENDIX I

The module must meet the following specifications:

(S) Electrical Specifications For L-Band T/R Module

Parameter	Specification
(1) Frequency (midband)	1.25 GHz
(2) Bandwidth (1 dB)	± 5% Frequency Agile; [20 MHz instantaneous signal.]
(3) DC Supply Voltage	Internal regulation and protection to be designated by contractor; however, the number of different potentials must be minimized along with their magnitudes. Internal energy supplies and/or regulators must be provided to meet the electrical requirements specified herein. In addition, a sufficiently rapid fail safe mode of operation must be achievable with the module so as to permit adjacent modules (connected to common outside dc buses) to continue to operate without degraded performance. Prime voltage supply buses outside the module are expected to be regulated ± 2% maximum.
(4) Power Output (min)	100W peak at antenna port including circuit, network, circulator-isolator and connector losses.
(5) Pulse Length	20 μsec min; 100 μsec max. (No pulse bursts)
(6) RF Power Input	100 mW or less, sufficient to maintain transmitter saturation at output with ± 1-dB variation in input level while meeting phase requirements specified herein.
(7) Duty Cycle (max)	1% fixed
(8) RF Interference	RF energy generated within the module and appearing on any power supply or logic lead to the transceiver module shall be at least 30 dB below the transmit output power level.

Parameter	Specification
(9) Antenna Port Load VSWR	50 ohms nominal; however module must survive a 5:1 VSWR, on an intermittent basis, while operating in either mode without damage. Unless otherwise noted, all performance specifications contained herein are based on a nominal 50 ohms antenna load.
(10) Receiver Noise Figure	4.0 dB max
(11) Overall Module Efficiency	35%; Goal = 40%
(12) Transmitter Efficiency (η_t)	40%; Goal = 45% including all circuit network transmission line isolator-circulator and connector losses; where: $$\eta_t = \frac{\text{Average } RF_{OUT}}{\text{Av } DC_{IN} + \text{Av } RF_{IN}}$$
(13) Transmitter Gain	30 dB MIN
(14) Spurious Intrapulse Transmitter Noise within signal band with RF drive present.	-35 dB maximum compared to module peak power power output
(15) Spurious oscillation during pulses with in any 0.5 MHz bandwidth from 0.5 GHz to 2.0 GHz (transmitter)	-50 dB maximum compared to module peak power output
(16) Allowable RF output amplitude droop during pulse (transmitter)	5.0% maximum at 1% duty cycle for 100-μsec pulse length
(17) Allowable transmit phase sensitivity to changes in DC supply voltages.	1 degree maximum cumulative output signal phase change
(18) Harmonic on transmit	The harmonic and out-of-band spurious outputs shall be down at least 50 dB from the 100 watts transmitter output
(19) Phase settling on transmit.	The output phase shall settle to within 5 degrees of nominal in less than 50 nsec after 10% to 90% rise time of amplifier.

Parameter	Specification
(20) Transmitter/Receiver Isolation	Sufficient isolation will be provided within the module so as to suppress regeneration between the transmitter and receiver independent of the mode of operation. In addition (for purposes of possible calibration) the reverse isolation between the antenna port and the RF input to the module shall be at least 35 dB down when transmitter/receiver switches are in transmit mode. When in receive mode, the reverse isolation between the RF input to the module and the antenna load port shall be 35 dB min.
(21) Reverse isolation between antenna port and transmitter final amplifier output in transmit mode.	Sufficient to prevent degradation of amp output power and/or reliability; $\geq$ 35 dB under varying antenna load VSWRs created by beam steering.
(22) Amplifier rise time (10% to 90%)	$\leq$ 50 nsec
(23) Phase Stability to temperature	$1^{o}/1^{o}$C Maximum (transmit or receive)
(24) Receiver Gain	25 dB minimum (antenna port to manifold port)
(25) Dynamic Range of receiver	1 dB compression at the output with -25 dBm maximum measured at input to module
(26) Transmitter Phase sensitivity per RF input power	$\pm 5^{o}$ for $\pm$ 1-dB change in RF drive level
(27) Allowable receiver phase sensitivity to changes in DC supply voltages	0.5^{o} maximum cumulative receiver output signal phase change
(28) Input receiver VSWR relative to 50 ohms	$\leq$ 1.4:1 at antenna input port of circulator/isolator relative to 50 ohms when module is in receive mode.
(29) Logic and T/R levels	Standard 5-volt TTL compatible logic shall be used in the module to drive the phase shifter and the TR switches.

Parameter	Specification
(30) Phase Shifter Logic/inputs	Provisions must be made in module to sum two serial 4 bit inputs and store in an accumulator register. Provisions will be made to transfer accumulator data into a driver storage register upon command by a transfer pulse.
(31) Phase Shifter Bits nominal at 1.25 GHz $\pm$ 5% frequency.	4 bits, 180^{o}, 90^{o}, 45^{o}, and 22.5^{o}.
(32) Differential module phase shift accuracy for any combination of bits and when connected to matched source or load (depending on whether in transmit or receive mode) in the manifold.	$\pm$ 10^{o} peak and 5^{o} RMS overall module error as measured for a line-length phase shifter which has an increasing linear phase with increase in frequency.
(33) Insertion Phase:	During Phase I, the contractor shall establish the absolute electrical length or insertion phase of the module in both modes of operation, and make necessary provision for adjustments in production in order to eliminate wave-length ambiguities, while at the same time meeting both the absolute and relative phase specifications and allowable deviation from linearity.
(34) Phase Shifter Logic Load Time	1.6 μsec maximum
(35) Phase Shifter Settling Time	0.5 μsec maximum from start of transfer pulse to settled phase shifter
(36) TR Switching Time	5 μsec maximum
(37) Clock Speed Max.	2.5 MHz; $\pm$ 5%
(38) Manifold Port VSWR	$\leq$ 1.5:1
(39) Transmit or receive intra-pulse phase linearity	1^{o} peak max. over specified instantaneous signal bandwidth located anywhere within agile band, with a change rate not exceeding 0.5^{o}/10 MHz
(40) Transmit or receive intra pulse amplitude linearity	0.5 dB max. over specified instantaneous signal bandwidth located anywhere within agile band.

Parameter	Specification
(41) Pulse-to-Pulse Phase and Amplitude Variations	For any successive quantity of six 100-μsec pulses, repeated at 1% duty cycle and operating over a 20-MHz instantaneous signal bandwidth, located at any fixed reference within the agile bandwidth, periodic phase variation about the mean shall not exceed 1^{o} peak. Under the same condition, amplitude variation about the mean pulse amplitude shall not exceed 0.2 dB peak. A periodic variation is defined as having a sinusoidal form, (including a damped sinusoid) of at least 2 full cycles.
(42) Transmitter and Receiver Phase tracking between modules over any 20 MHz within the 1-dB bandwidth	12^{o} RMS*; 17^{o} peak
(43) Transmitter P_o and receiver gain tracking between modules over any 20 MHz within the 1-dB bandwidth	1.0 dB RMS*
(44) Quadratic Phase Error in Transmit or Receive:	During any 20-MHz instantaneous signal bandwidth (center and edges included) the quadratic phase error shall not exceed 15 degrees. Straight line reference for each pair of measured data have no relationship to each other. Receive measurements can be made in CW mode. Transmitter evaluated in 100-μsec pulsed mode at 1% duty.

*RMS tracking for subsequent production quantities is defined as follows: For shippable quantities less than the total lot procurement, the mean and standard deviation will be calculated by the contractor for all modules heretofore produced, and the subject group to be shipped will fall within the limits specified.

REFERENCES

1. *RCA, Moorestown, Phase I Task 2 MA 002670, 31 May 74, Solid State Transmit Receive Module.

2. *MA, Burlington, Mass, Final Engineering Report, BP1095, Phase I Task II, Solid State XMT RCV Module, July 1974.

3. A. I. Zutkoff, "L-Band, Solid-State Transmit/Receive Module, Phase-I Final Report," NRL Report 7873, May 8, 1975 (Secret).

* Phase I, Task II in contractor terminology is equivalent to NRL reference to Phase II.